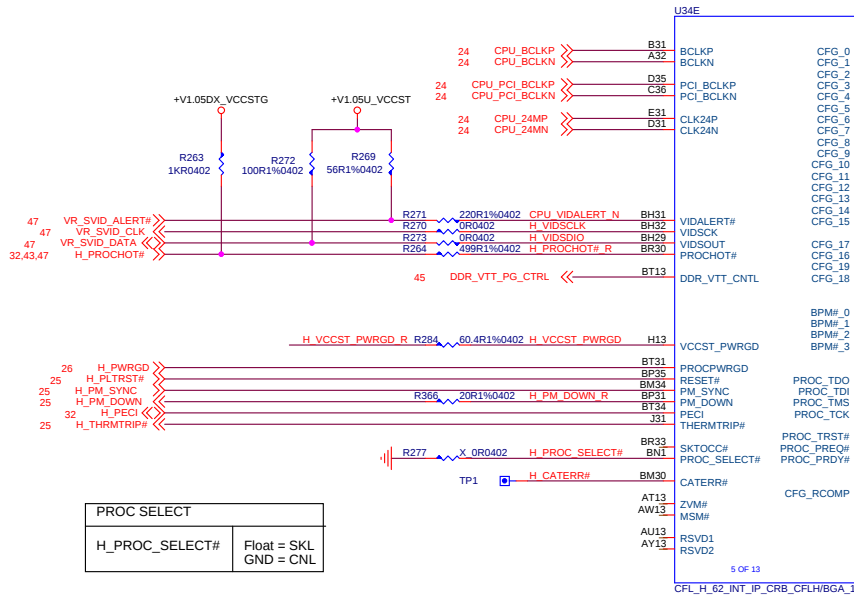
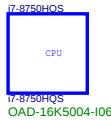
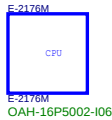
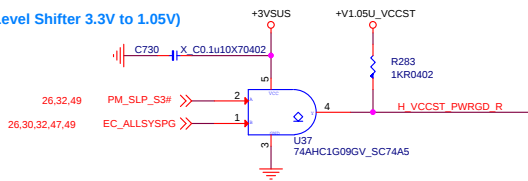




VCCST_PWRGD

(Level Shifter 3.3V to 1.05V)



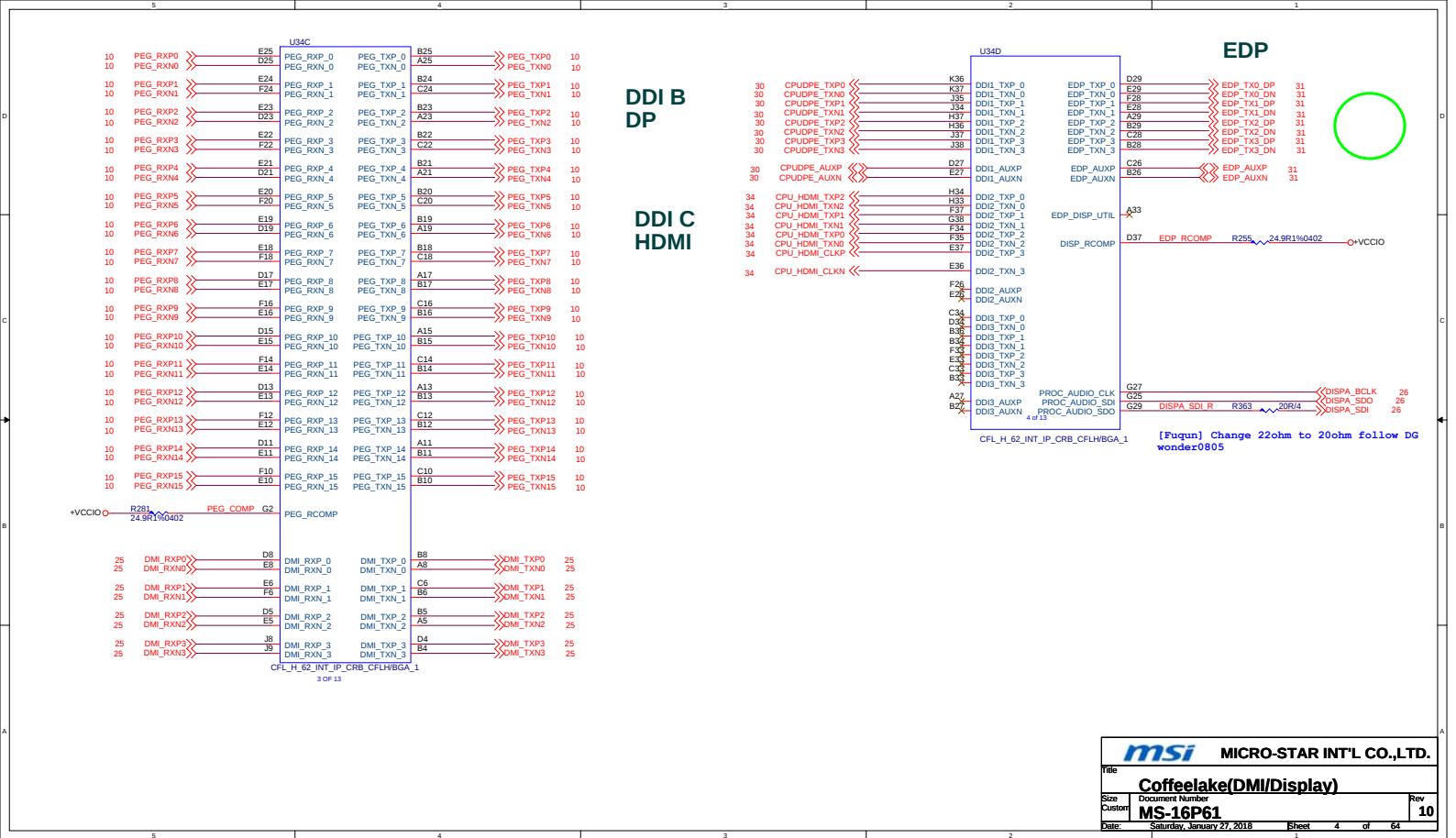
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	1 = (Default) Normal Operation; No stall 0 = Stall
PCI Express * Static X16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.
eDP Enable	
CFG4	1 = Disabled 0 = Enabled
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
PEG DEFER TRAINING	
CFG7	1: (default) PEG Train immediately following RESET# de assertion. 0: PEG Wait for BIOS for training

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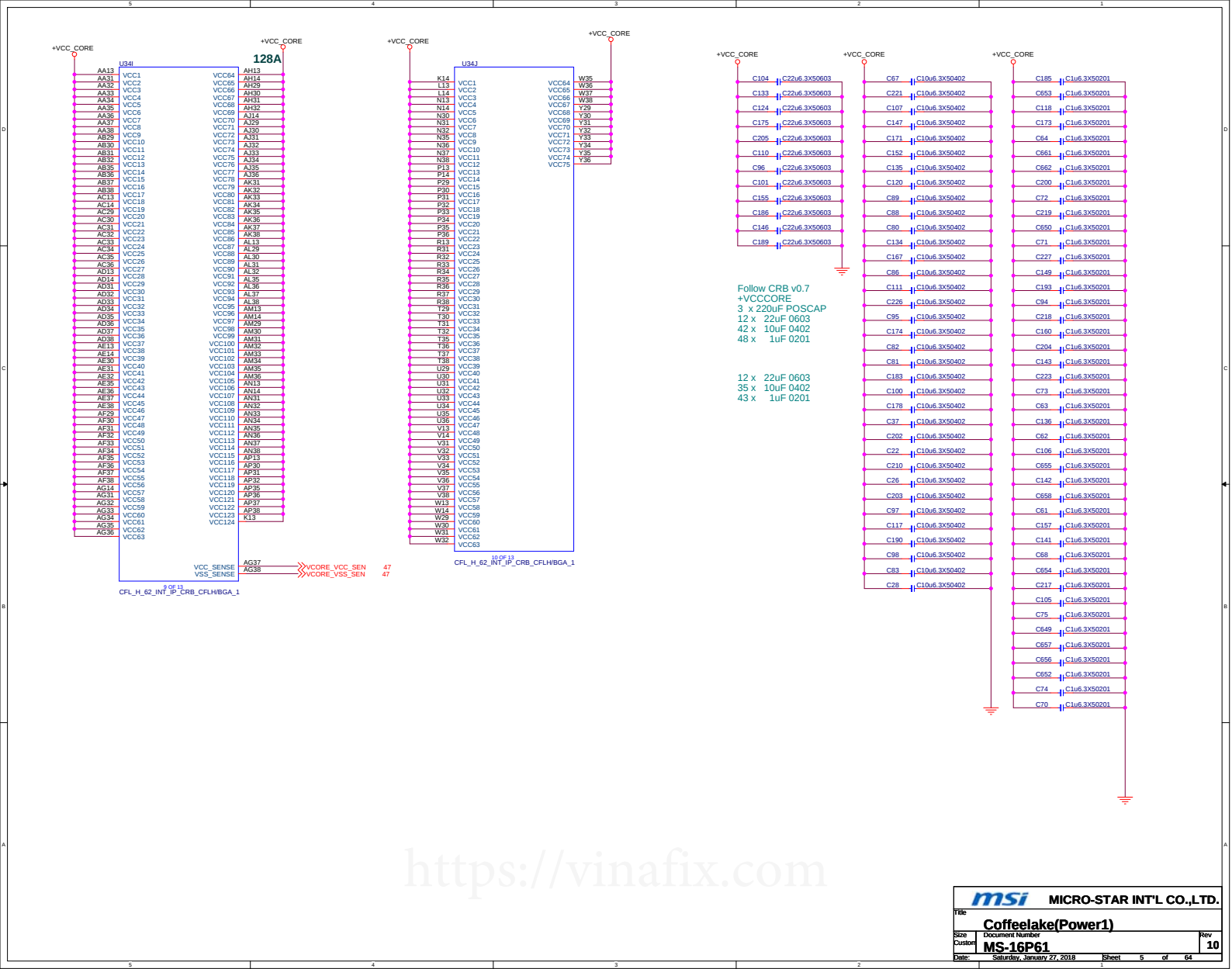
msi MICRO-STAR INT'L CO.,LTD.	
Title	
Coffeelake(HOST)	
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DDR Channel B

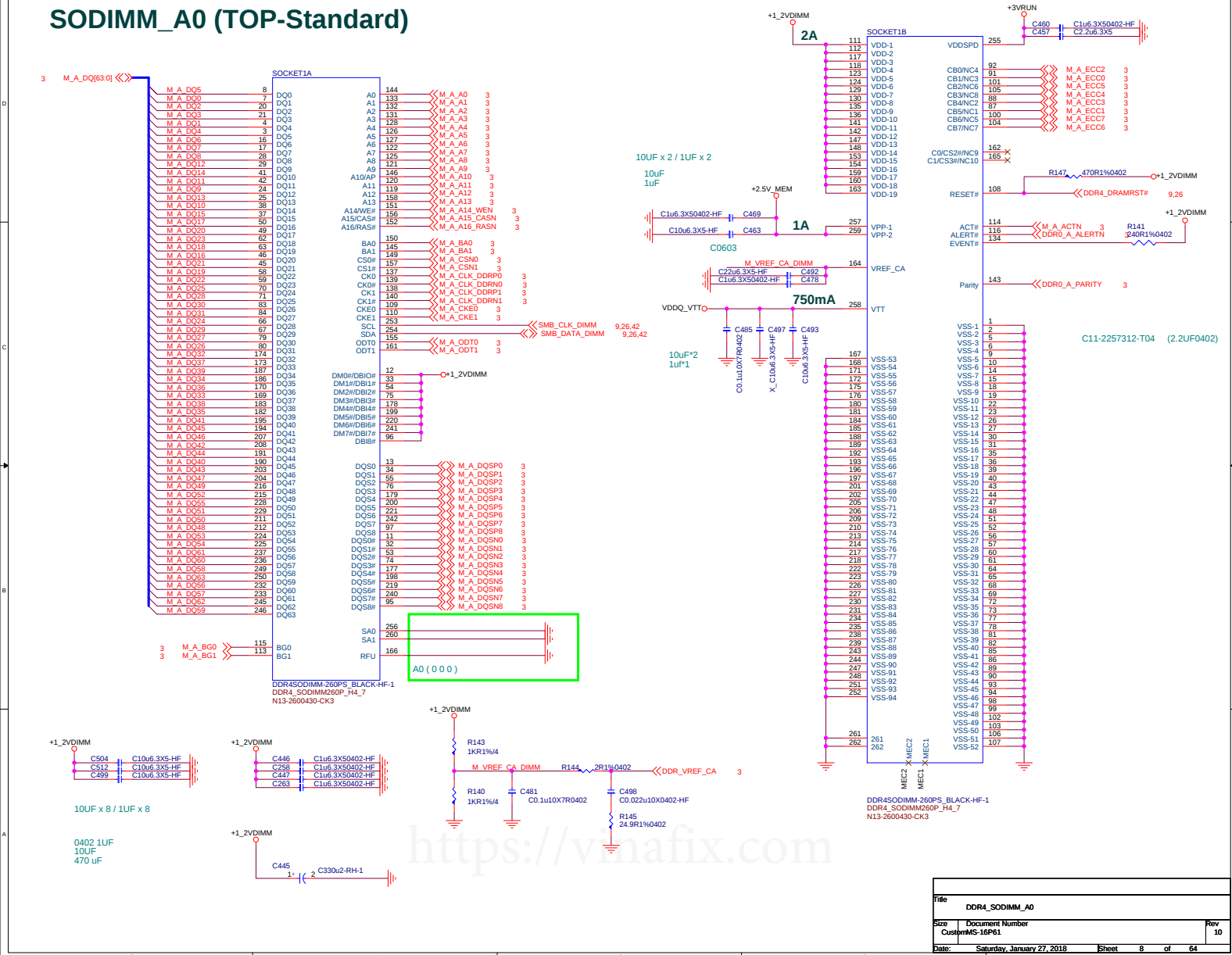




<https://vinafix.com>



SODIMM_A0 (TOP-Standard)

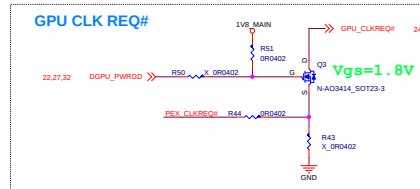


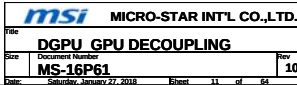
Title			
DDR4_SODIMM_A0			
Size	Document Number	Rev	
Custom	MS-16P61	10	
Date:	Saturday, January 27, 2018	Sheet	8 of 64

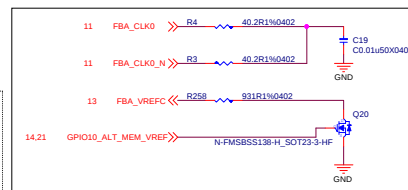
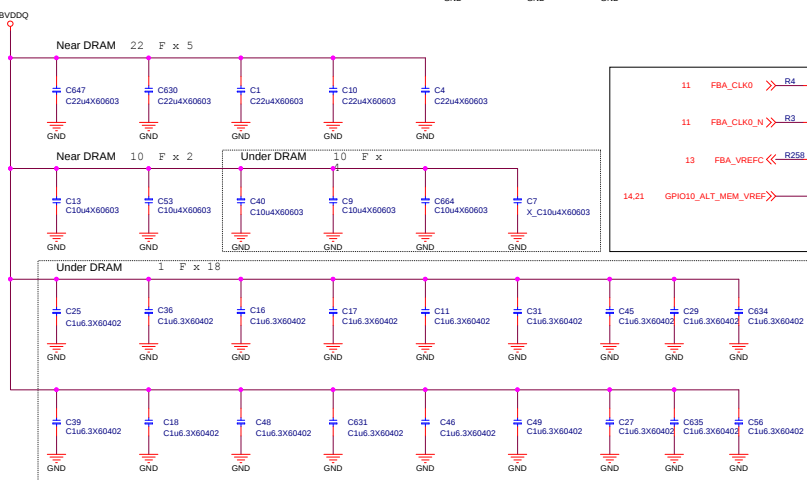
Vinafix.com

Title			
DDR4_SODIMM_B0			
Size	Document Number	Rev	
Custom	MS-16P61	10	
Date:	Saturday, January 27, 2018	Sheet	9 of 64

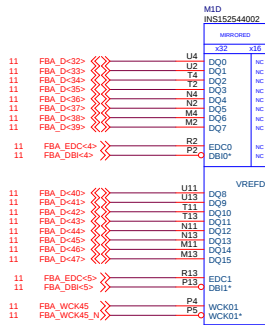
https://vinafix.com



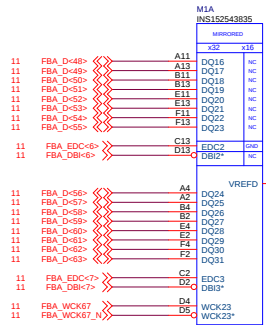




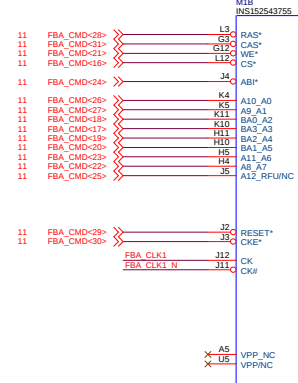
DGPU_GDDR5 FrameBuffer A1



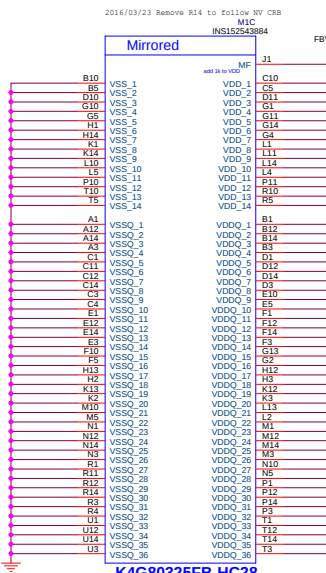
K4G80325FB-HC28



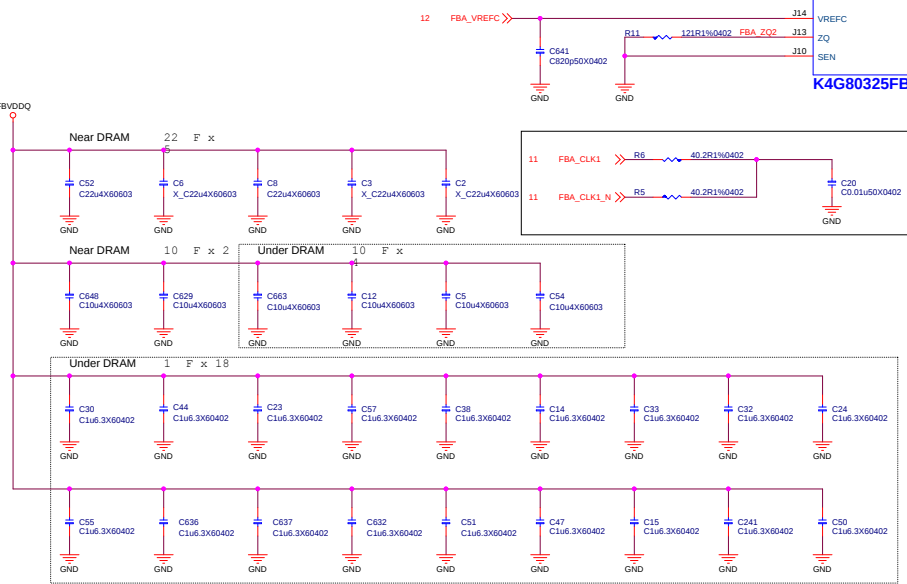
K4G80325FB-HC28



K4G80325FB-HC28

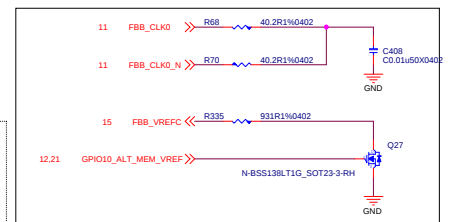
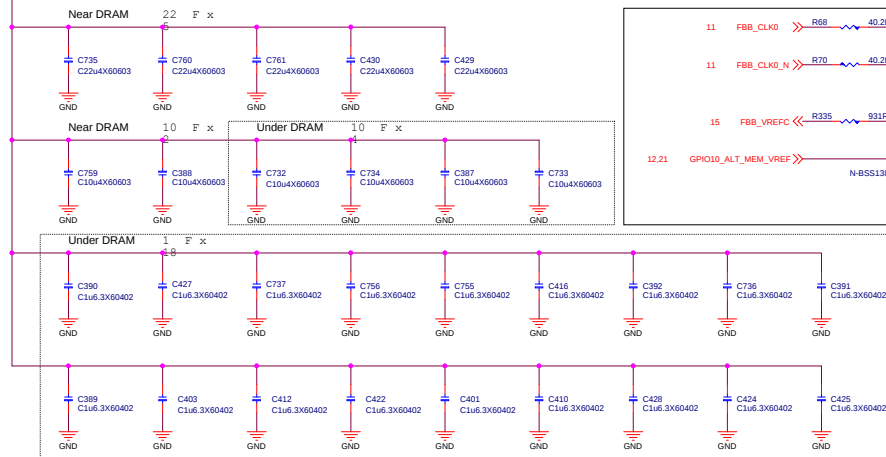


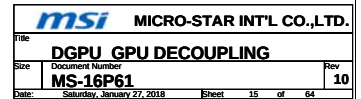
K4G80325FB-HC28



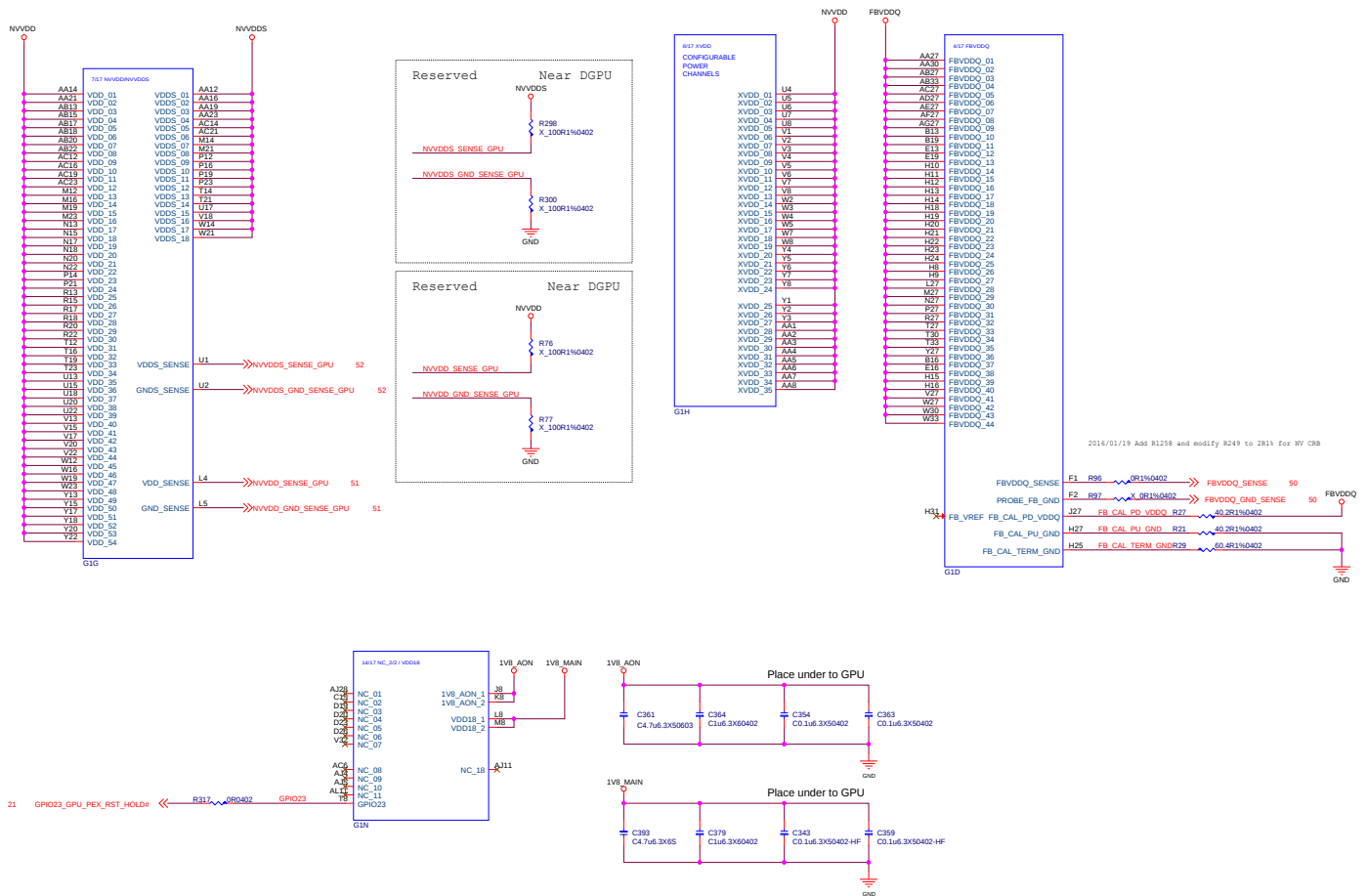
<https://vinafix.com>

msi		MICRO-STAR INT'L CO.,LTD.	
File			
DGPU_GPU DECOUPLING			
Size	Document Number	Rev	
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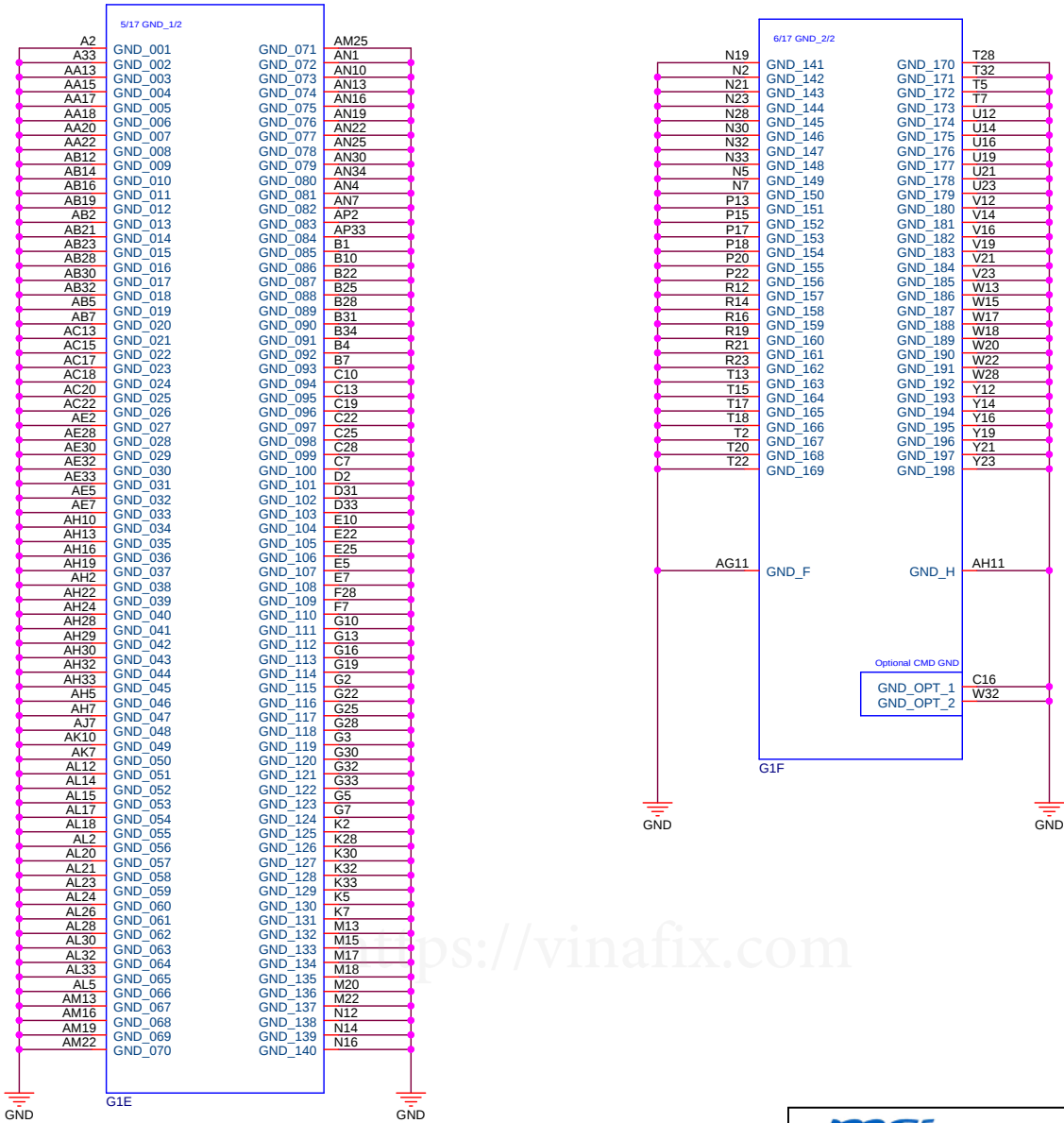


GPU NVVDD, FBVDDQ



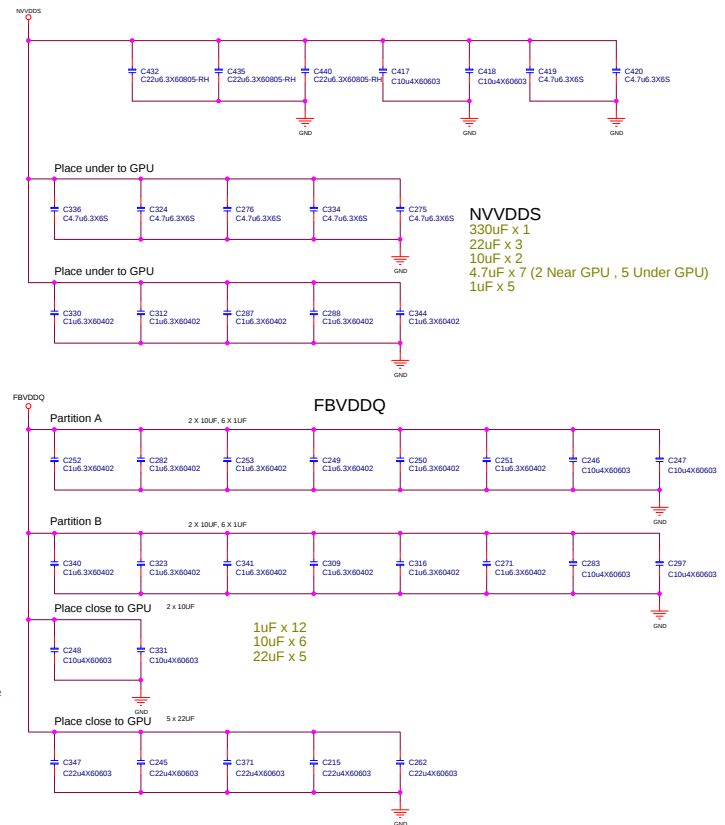
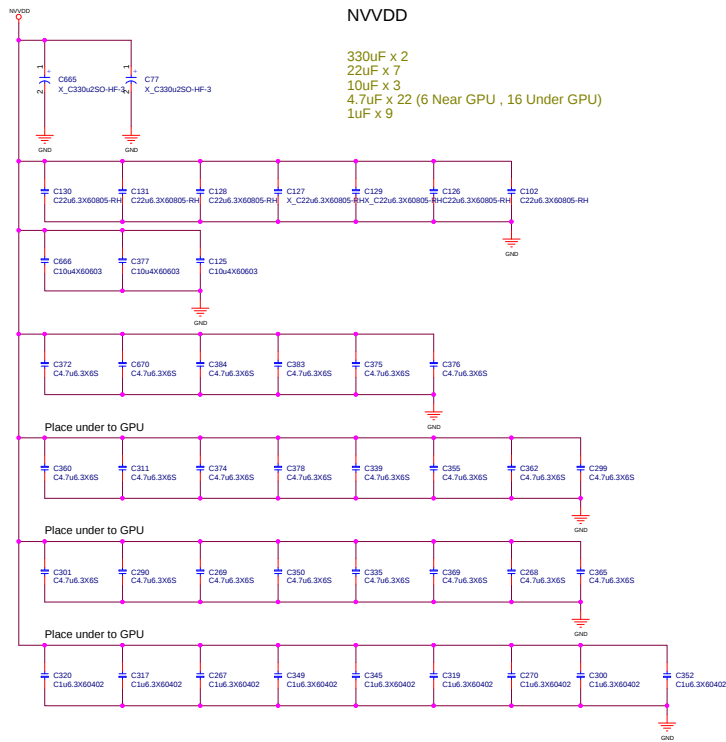
<https://vinafix.com>

DGPU GND



msi MICRO-STAR INT'L CO.,LTD.		
Title		
DGPU GPU DECOUPLING		
Size	Document Number	Rev
	MS-16P61	10
Date:	Saturday, January 27, 2018	Sheet 17 of 64

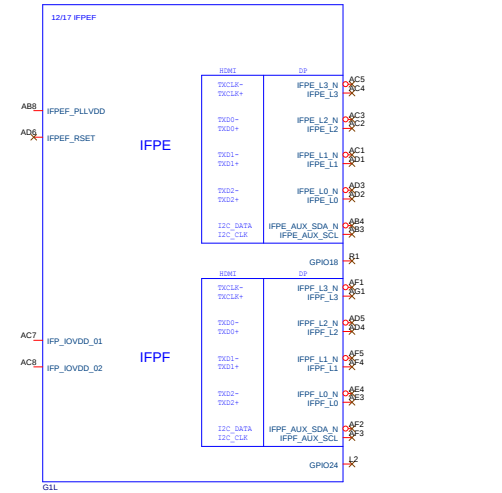
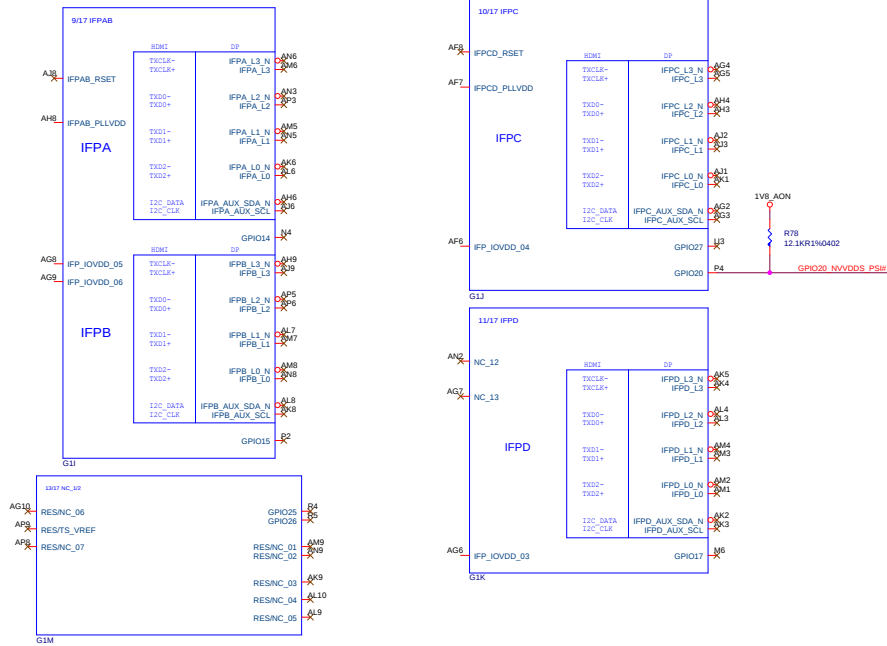
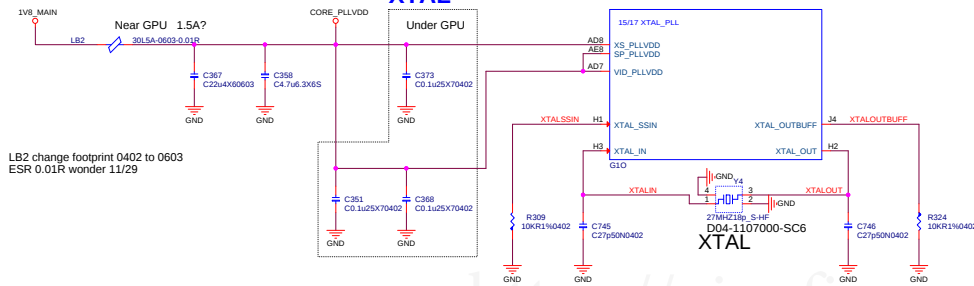
GPU DECOUPLING



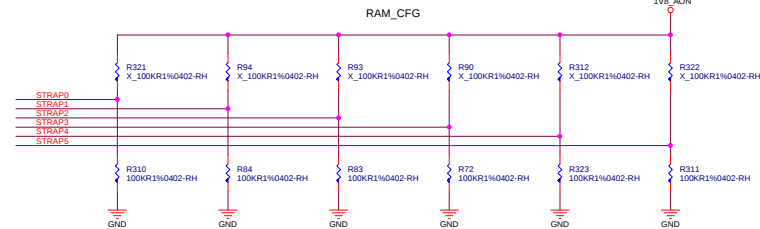
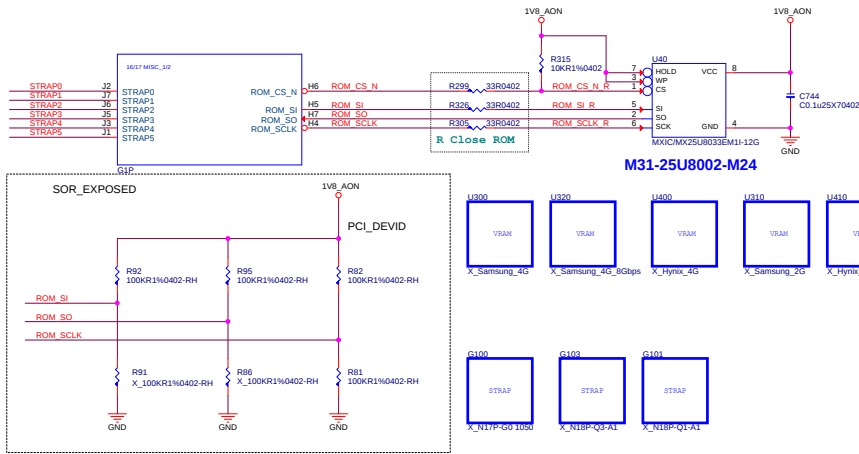
msi MICRO-STAR INT'L CO.,LTD.			
File	DGPU_GPU DECOUPLING		
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DACA, Display IF

DGPU
XTAL

ROM, MULTI-LEVEL STRAPS



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: M12-80325A5-S02 / K4G80325FB-HC28 4GB	R310 R84 R83
L	L	H	0x1 Micron: MT51J256M32HF-70-A	R310 R84 R93
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	R310 R94 R83
L	H	H		
H	L	L		
H	L	H		
H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	R321 R94 R83
H	H	H	0x7 Samsung: M12-41325A5-S02/K4G41325FE-HC28 2GB	R321 R94 R93
L	L	M	0x8 Micron: EDW032BABG-70-F-A	R310 R84 R93R83
L	M	L		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

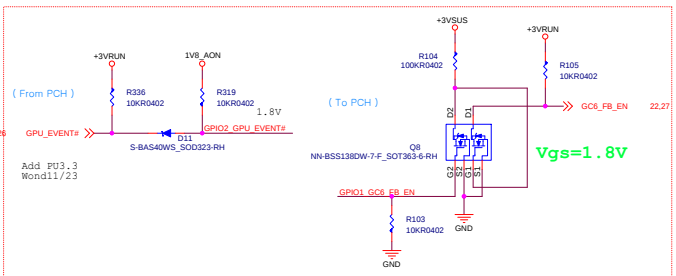
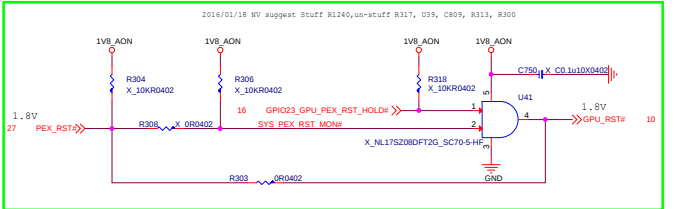
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

<https://vinafix.com>

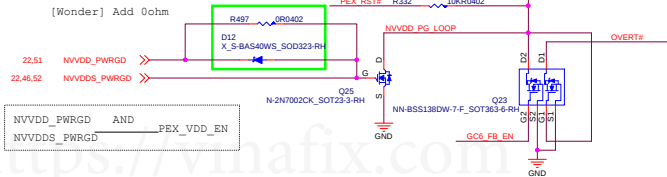
NVVDD_PWRGD AND
 NVVDS_PWRGD PEX_VDD_EN

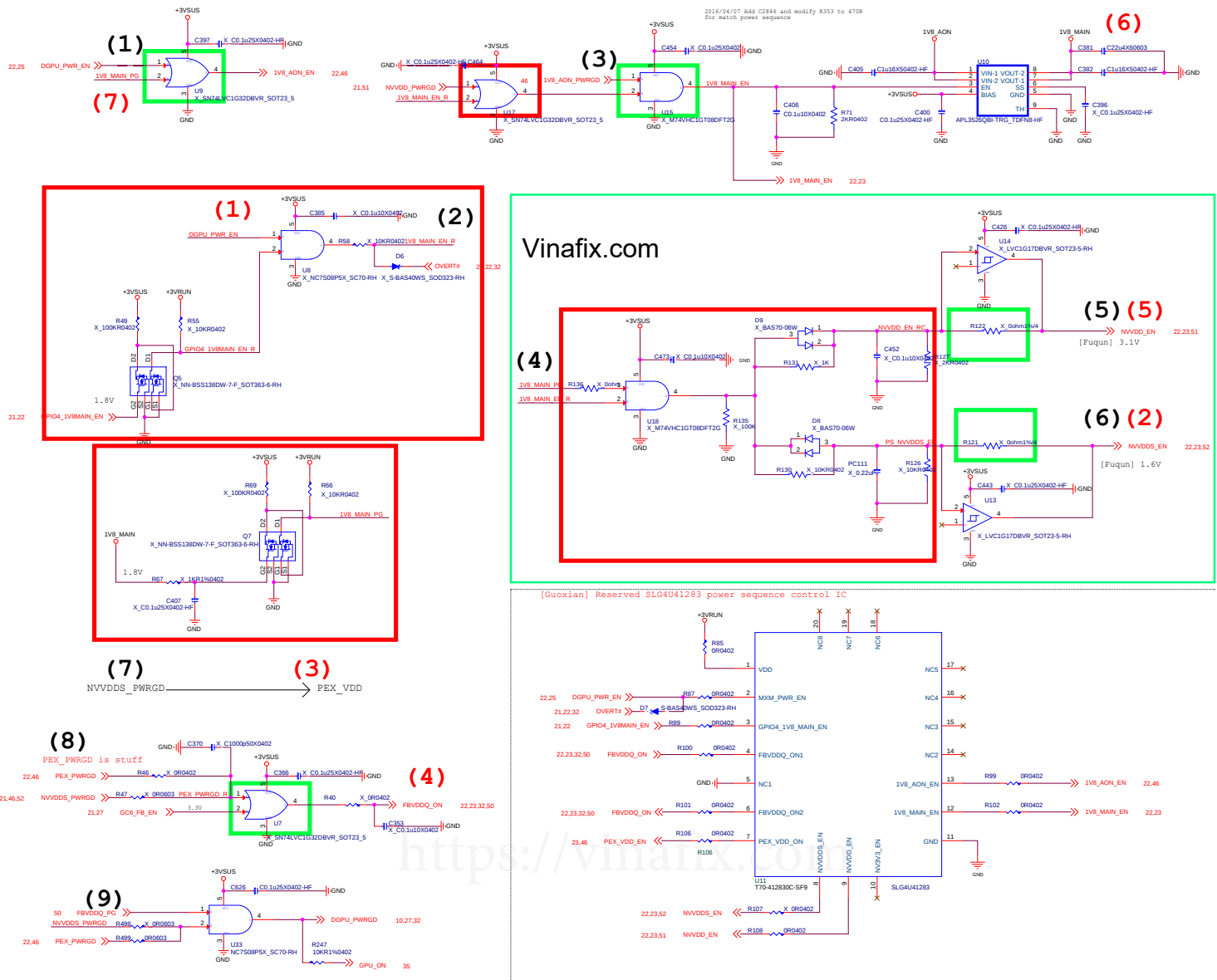
GND

GC6_FB_EN



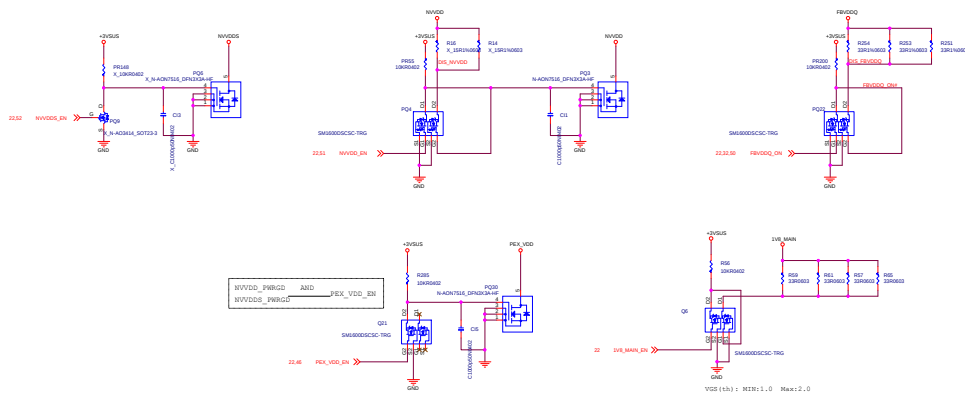
[Wonder] Add 0ohm



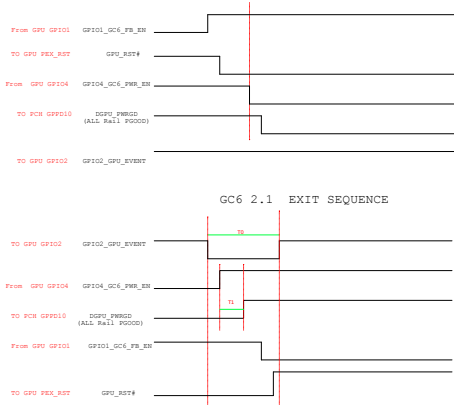


Discharge

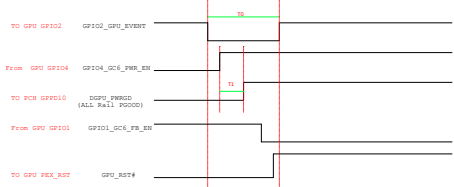
Remove NVVDS Power IC
F1148 PQ9 PQ9, C13



GC6 2.1 ENTRY SEQUENCE



GC6 2.1 EXIT SEQUENCE



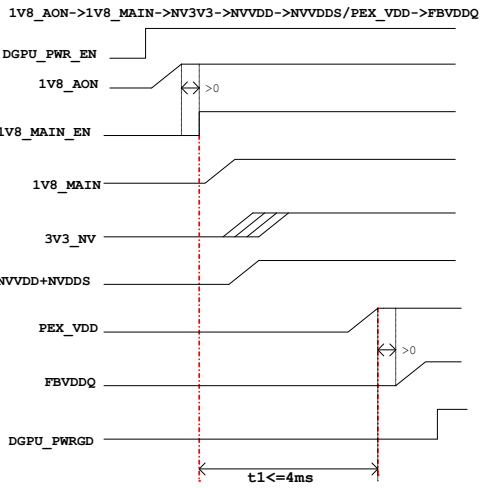
GC6 2.1 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	ms	GPU EVENT# assertion
T1	0.04	4	ms	3V3 MAIN EN assertion to all power rails up and stable

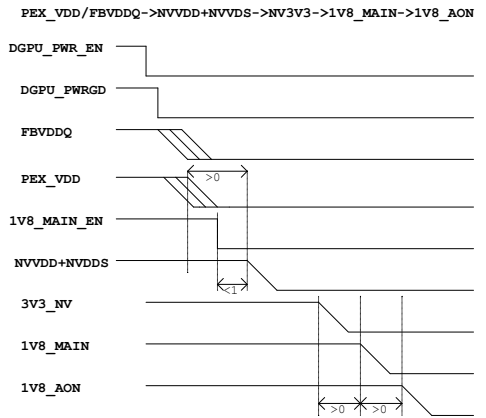
NOTES:

1. All RailPGOOD=1 represents all GPU power rails are ramped up and in regulation.
If any GPU power rail cannot go guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

POWER UP Sequence



POWER Down Sequence



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EPF LED

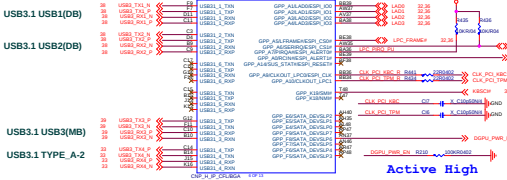
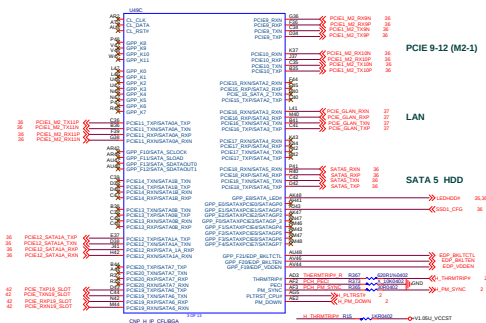


USB 2.0	USB 3.1	Device	Note
1	1	USB TYPE C-1	
2	2	USB TYPE C-2	
3	3	USB TYPE A-1	
4	4	USB TYPE A-2	
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			

GPIO
External pull-up is required. Recommend 200K.
This signal should sample HIGH. There should NOT be any on-board device driving to opposite direction during sleep sampling.

High Speed I/O Ports	Device
1	USB3.1 Gen1
2	USB3.1 Gen1
3	USB TYPE A-1
4	USB TYPE A-2
5	INTEL LAN Only
6	PCIe
7	PCIe
8	PCIe
9	PCIe
10	PCIe
11	PCIe
12	PCIe
13	PCIe
14	PCIe
15	PCIe
16	PCIe
17	PCIe
18	PCIe
19	PCIe
20	PCIe
21	PCIe
22	PCIe
23	PCIe
24	PCIe

SATA Lane 0 has the flexibility to be mapped to PCIe 11 or 13
SATA Lane 1 has the flexibility to be mapped to PCIe 12 or 14



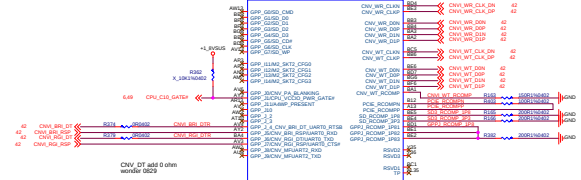
GPIO
External pull-up is required. Recommend 200K.
This signal should sample HIGH. There should NOT be any on-board device driving to opposite direction during sleep sampling.

GPP_A6
PCI Interrupt Request A6
Note: An external Pull-up is required

GPP_A7
PCI Interrupt Request A7
Note: An external Pull-up is required

GPP_A14
LPC Mode - Suspend Status
The signal is asserted by the PCH to indicate that the system will be entering a low power sleep mode.

GPP_A15
LPC Mode - Suspend Status
The signal is asserted by the PCH to indicate that the system will be entering a low power sleep mode.



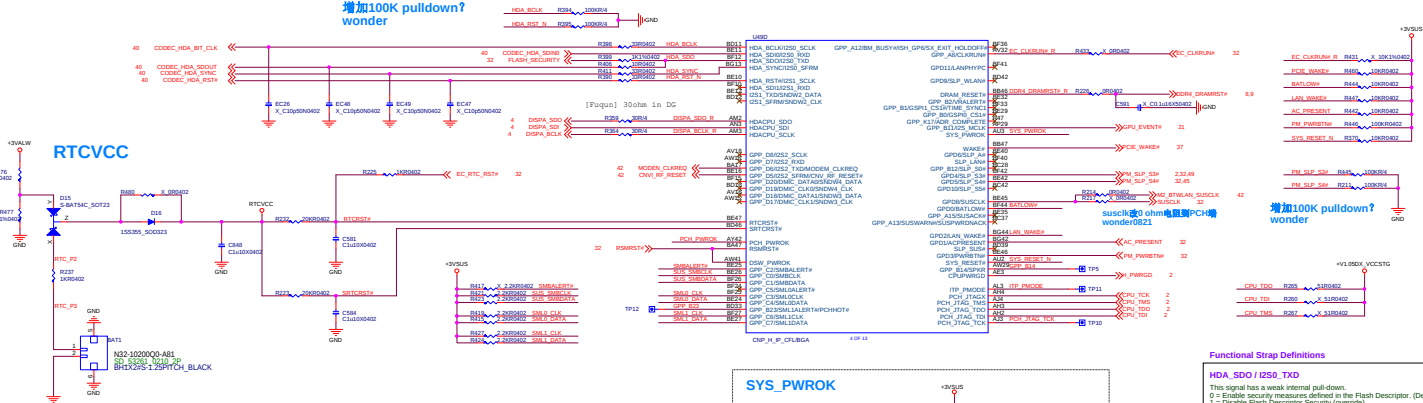
CNL PCH-H Preliminary HSIO Lane Assignments



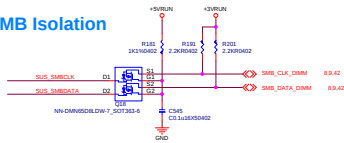
- Added 4 new PCIe 3.0 lanes across X8M-H platform.
- Gate LAN removed from lane 10 and SATA M.2 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

HM370 (HDA/RTC/SMBUS)

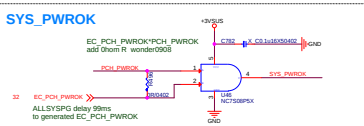
增加100K pulldown?
wonder



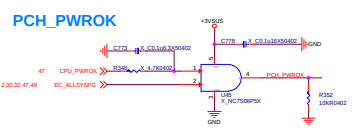
SMB Isolation



SYS_PWROK



PCH_PWROK



Functional Strap Definitions

HDA, SDO / I2S0, TXD
This signal has a weak internal pull-down.
0 = Enable Intel ME CRYPTO Transport Layer Security (TLS) cipher suite (for confidentiality). (Default)
1 = Disable Flash Descriptor Security (overmode).

SMBALERT# / GPP_C2
This signal has a weak internal pull-down.
0 = Disable Intel ME CRYPTO Transport Layer Security (TLS) cipher suite (for confidentiality). (Default)
1 = Enable Intel ME CRYPTO Transport Layer Security (TLS) cipher suite (both confidentiality). Must be pulled up to support Intel AMT with TLS.

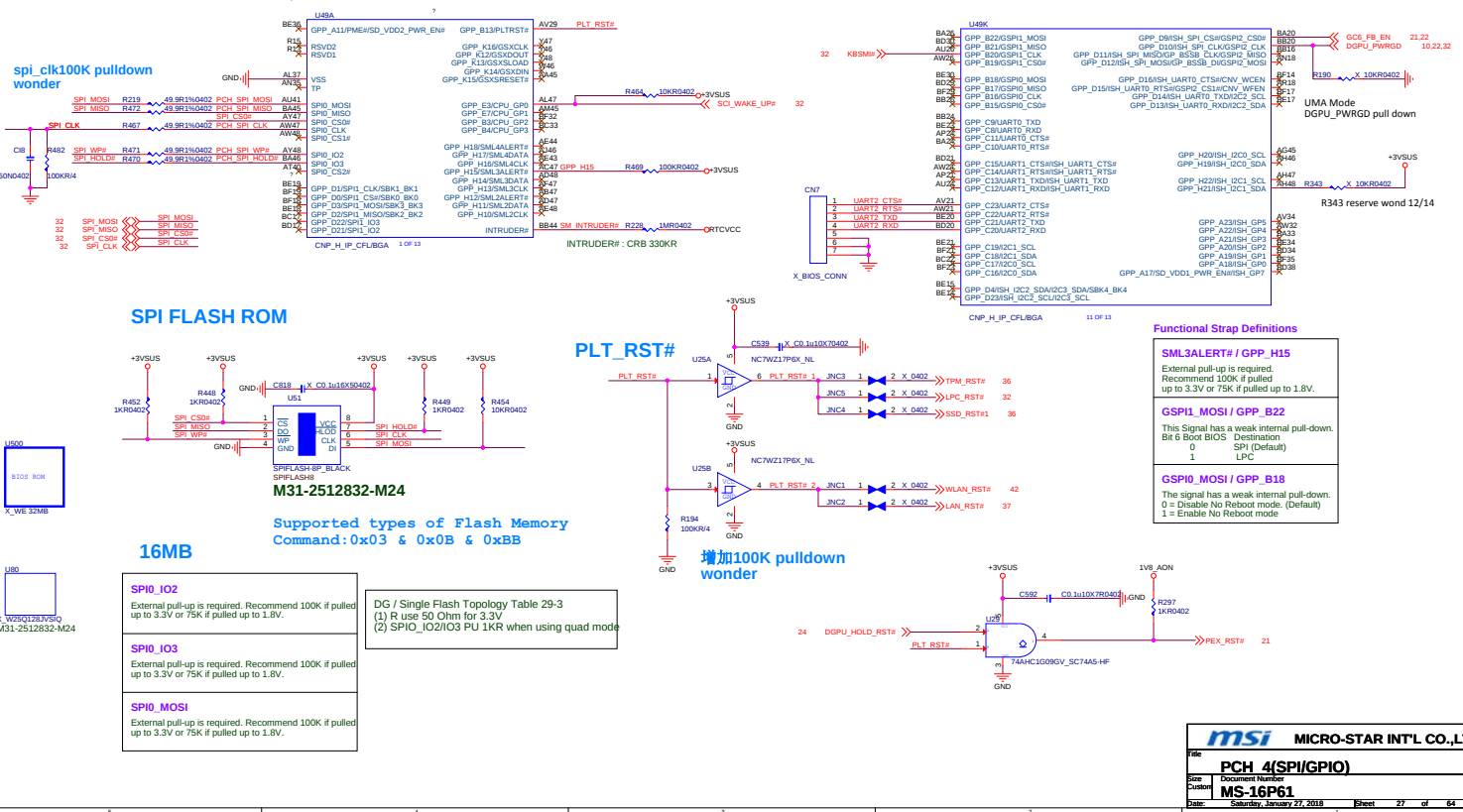
SMBALERT# / GPP_C5
This signal has a weak internal pull-down.
0 = Disable Intel ME CRYPTO Transport Layer Security (TLS) cipher suite (for confidentiality). (Default)
1 = eSPI is selected for EC.

SMBALERT# / PCHNOT# / GPP_B23
This signal has an internal pull-down.
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB

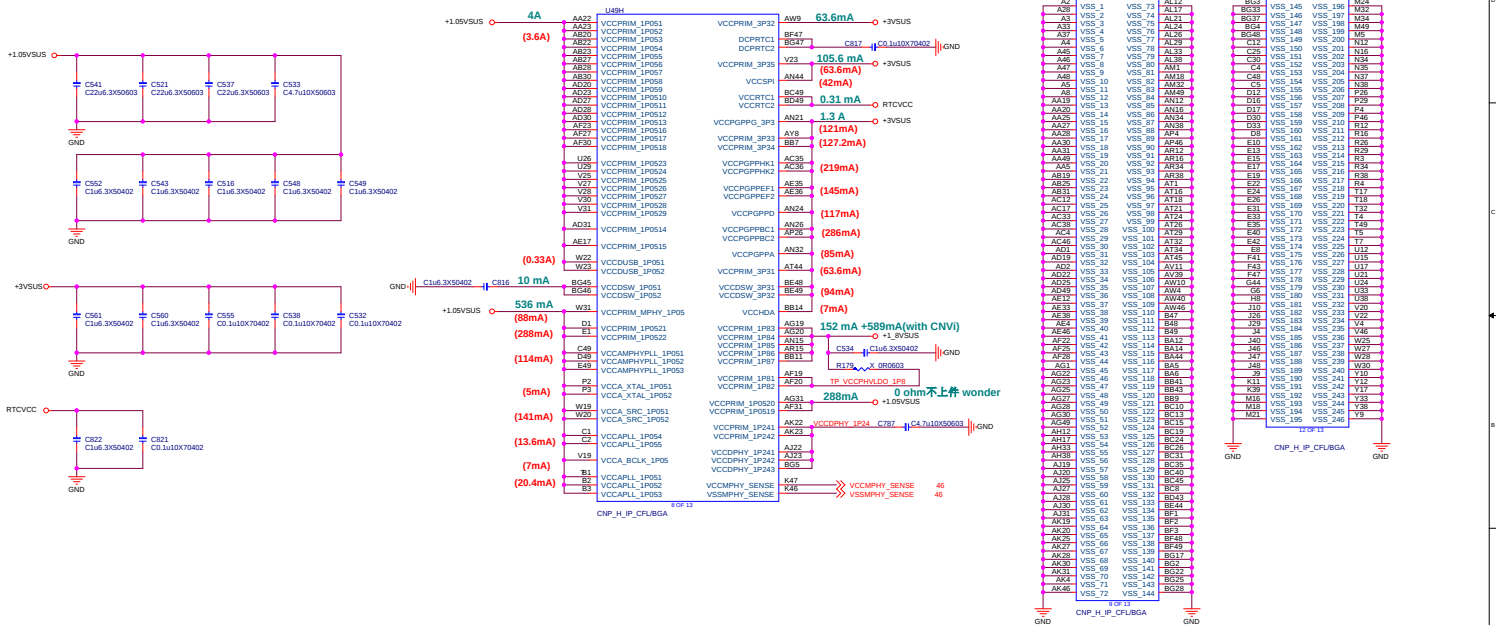
SPKR# / GPP_B14
The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode.

DG/ RTC Well Input Strap
RTCRST# & DSW_PWROK, PCH_PWROK - PD
RTCRST#, SRTCST#, INTRUDERS - PU

HM370 (SPI/GPIO)

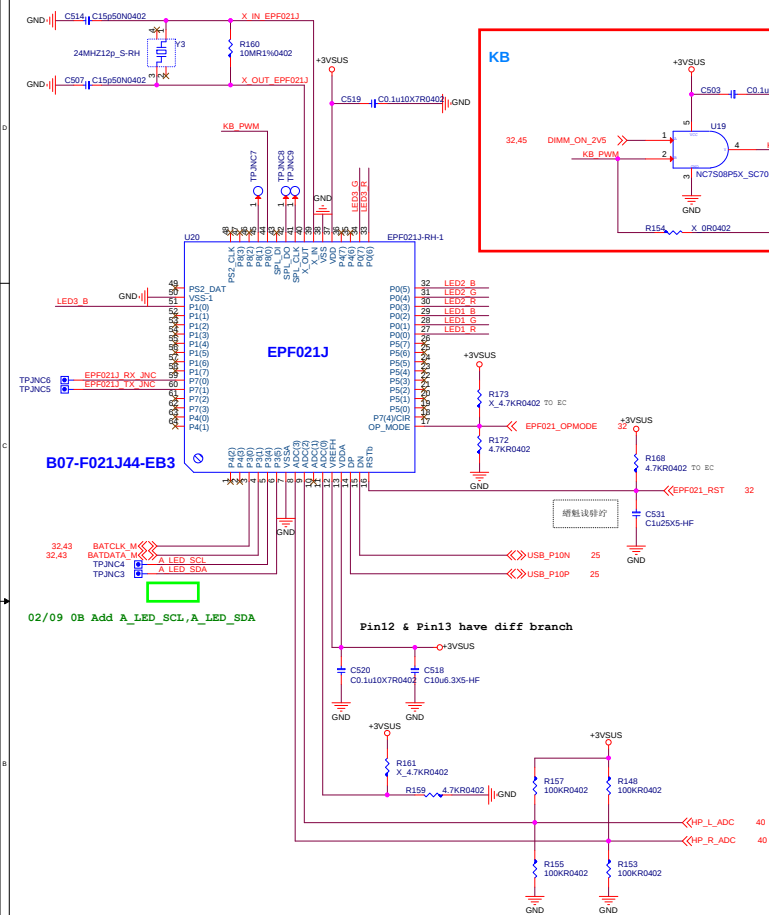


HM370 (Power & GND)

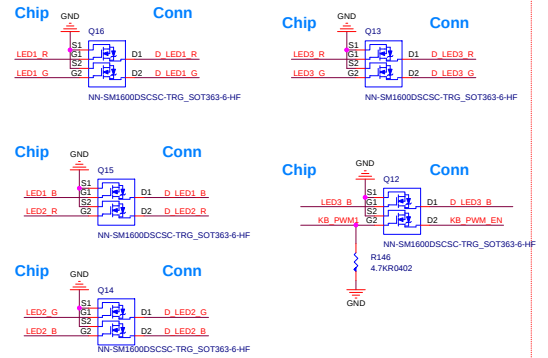


<https://vinafix.com>

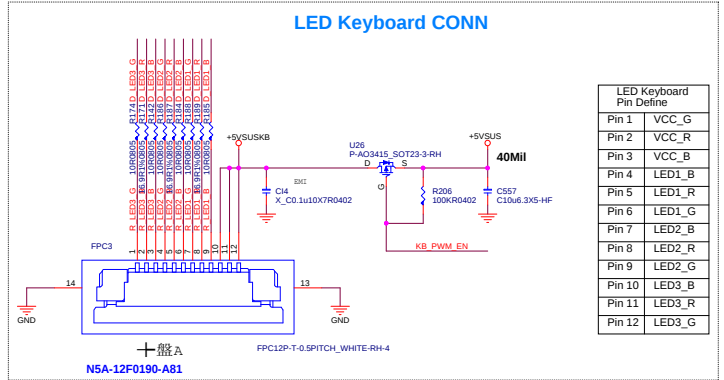
LED 8051 Controller



EPF021J Sink current not enough, only using BSS138 (0.22A)

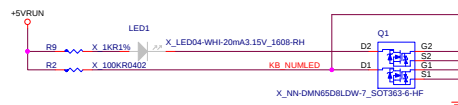


LED Keyboard CONN



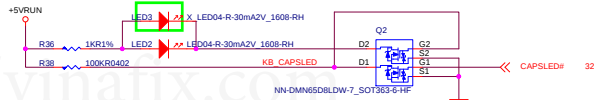
5/11 1.0 Remove 8051 KB LED control .

NUMLED预留



CAPSLED

16P6 LED2
17C6 LED3



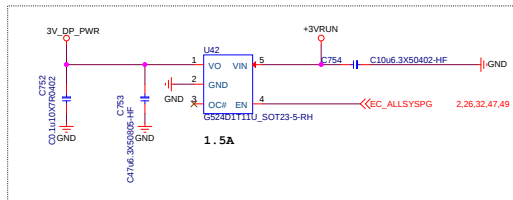
WELED
X_WHITE: 20mA

	LED2, LED3
GP, GL	D0C-0402010-L05
WE	D0C-040C300-L05

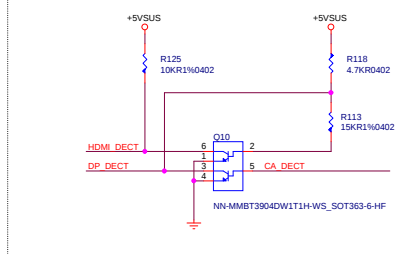
File	LED 8051KB CON
Size	Document Number
Customer	MS-16P61
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Display Port

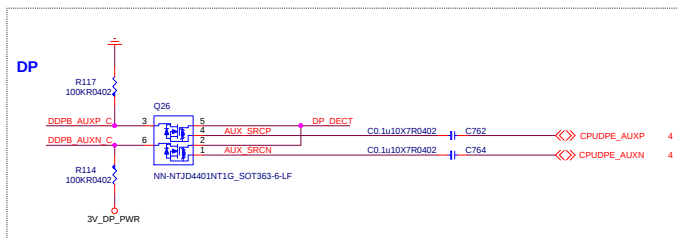
The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



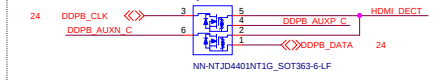
Display Select



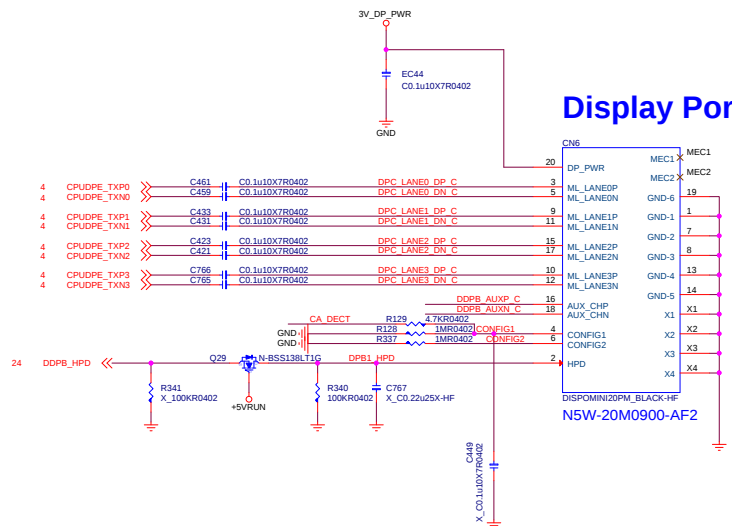
Dual Mode Switch



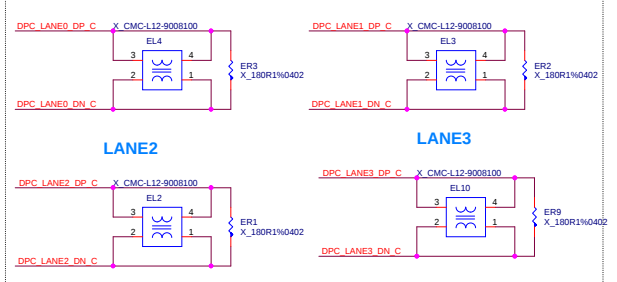
HDMI



Display Port



EMI Close Connector

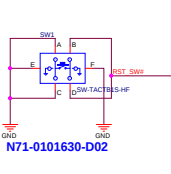


msi MICRO-STAR INT'L CO.,LTD.			
File	DP	Document Number	MS-16P61
Size		Rev	10
Date	Samudra, January 27, 2018	Sheet	30 of 64

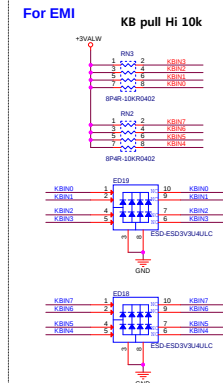
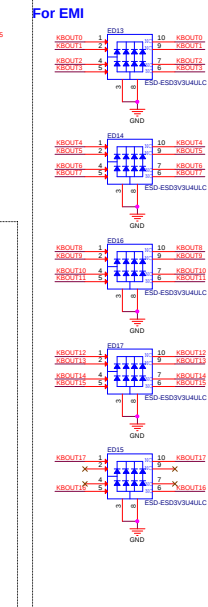
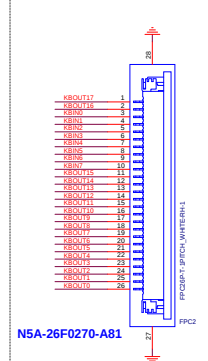
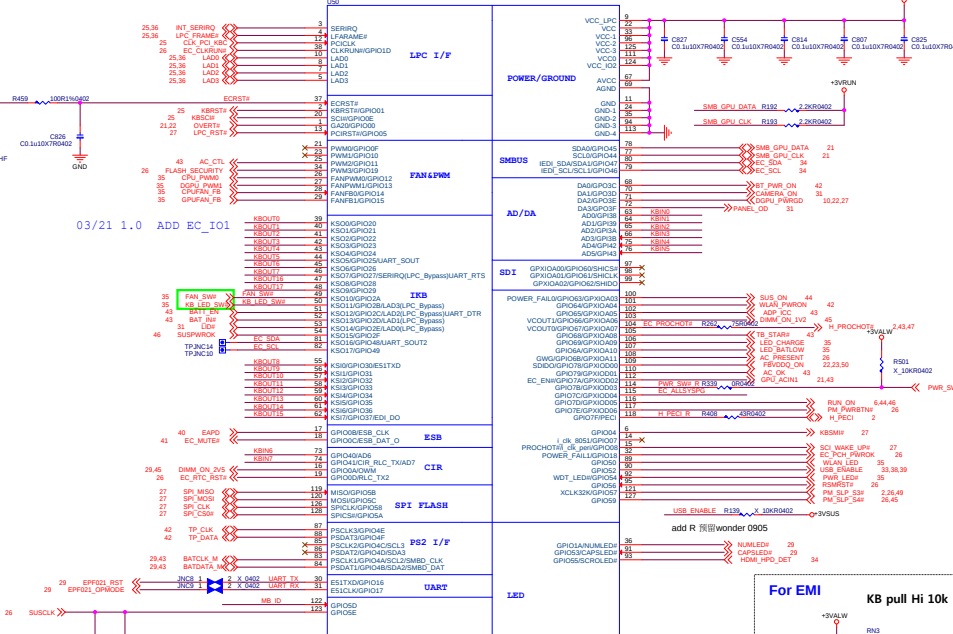
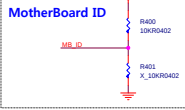
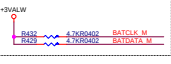
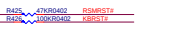
<https://vinafix.com>

BBC/EC/uP (ENE9028)

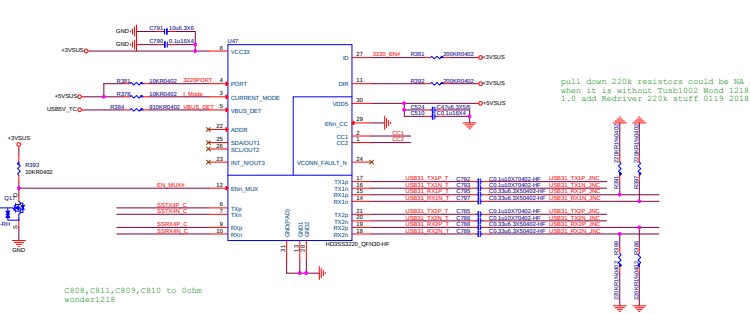
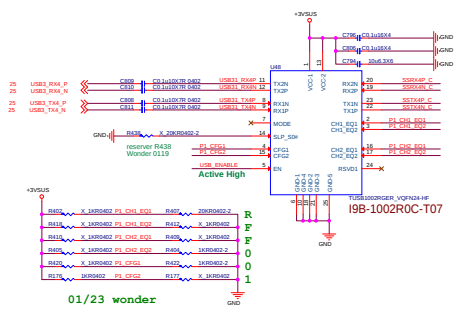
Hardware Reset



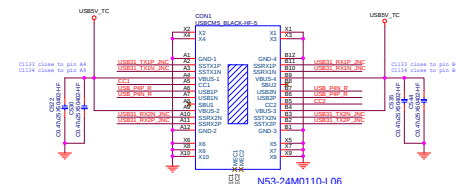
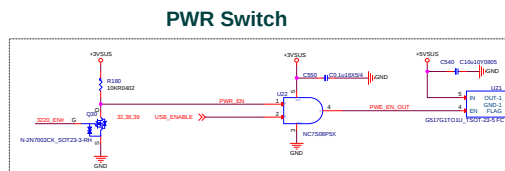
PU/PD



USB3.1 TYPE C



Type-C Connector

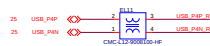


Port =1 (DFP mode)
Current_Mode =1 (3A)
ADDR= NC (GPIO mode)
ENa_MUX=0 (Enable)
ENa_CC=0 (Enable CC Controller)
ID: OD output =0 when CC pin detected device attachment

ESD



USB20 CMC



<https://vinafix.com>

Doc Number	MS-1001	Rev	1.0
Doc Name	MS-1001	Doc Date	2018/07/27
Doc Ver	1.0	Doc Rev	1.0

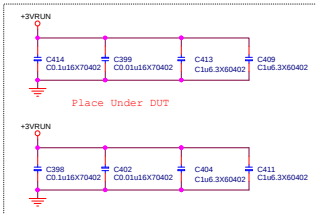
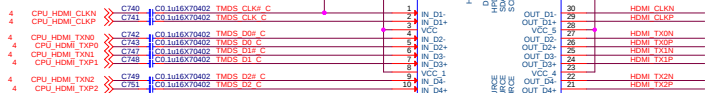
HDMI Level Shifter

HPD_SNK Internal PD 130kohm

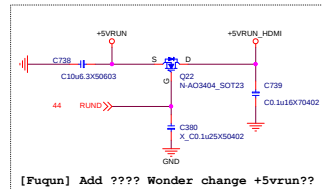
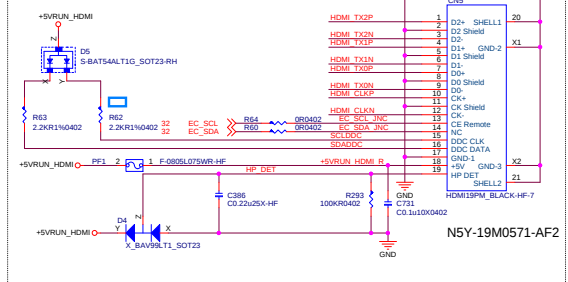
ESD 10KV

HP DET
PULSED
UNPLUGGED
5V
0V

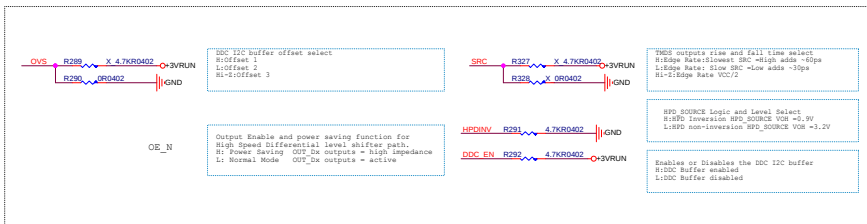
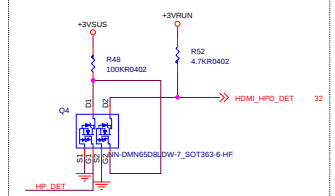
V1.0 reserved for
ADC TV issue.



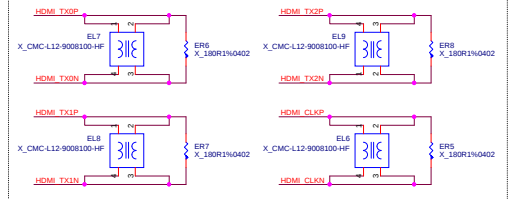
HDMI Connector



HPD Level Shift 5V to 3V



EMI



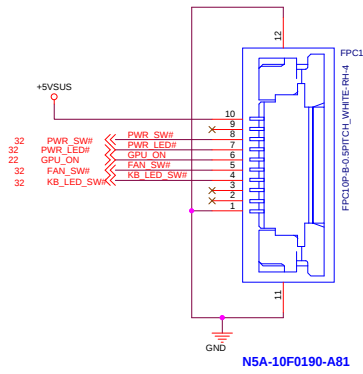
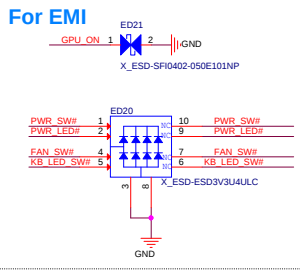
msi MICRO-STAR INT'L CO.,LTD.	
File	HDMI DP139
Size	Document Number
16P61/17C61	Rev 10
Date	Saturday, January 27, 2018
Sheet	34 of 64

<https://vinafix.com>

Power Switch Connector

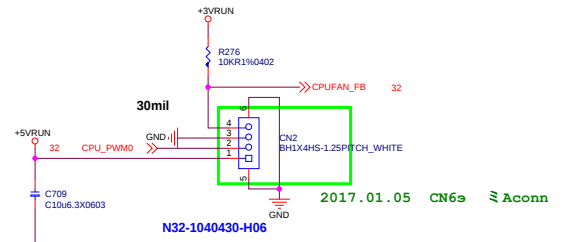
CPU FAN/GPU FAN/POWER Switch

For EMI



N5A-10F0190-A81

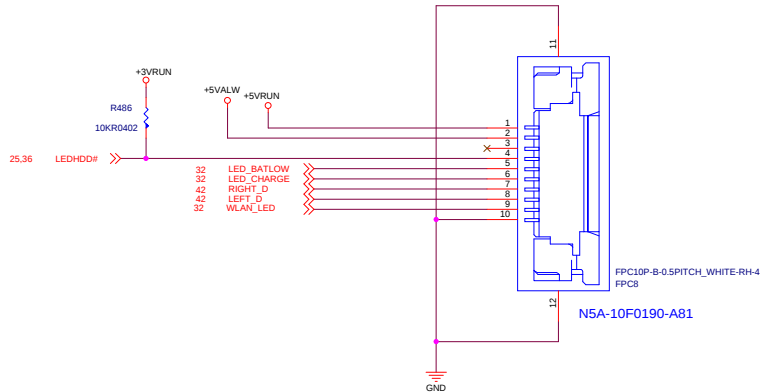
CPU FAN



N32-1040430-H06

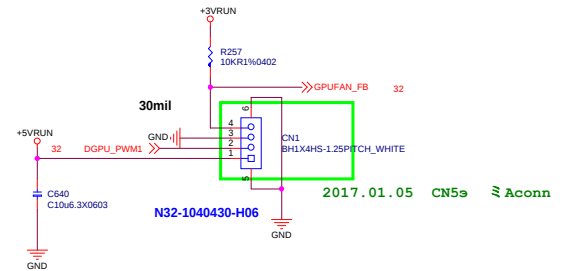
2017.01.05 CN69 Aconn

Switch connector



N5A-10F0190-A81

DGPU FAN



N32-1040430-H06

2017.01.05 CN59 Aconn

msi MICRO-STAR INT'L CO.,LTD.			
File	CPU FAN/BTB CONN/LED		
Size	Document Number	Rev	
Custom	MS-16P61	10	
Date	Saturday, January 27, 2018	Sheet	35 of 64

<https://vinafix.com>

[illegible]

40	NC	No Connect
41	SATA-B+/PEr0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PEr0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A+/PET0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A-/PET0	Host transmitter differential signal pair

[illegible]

N5N-22F0401-AF2

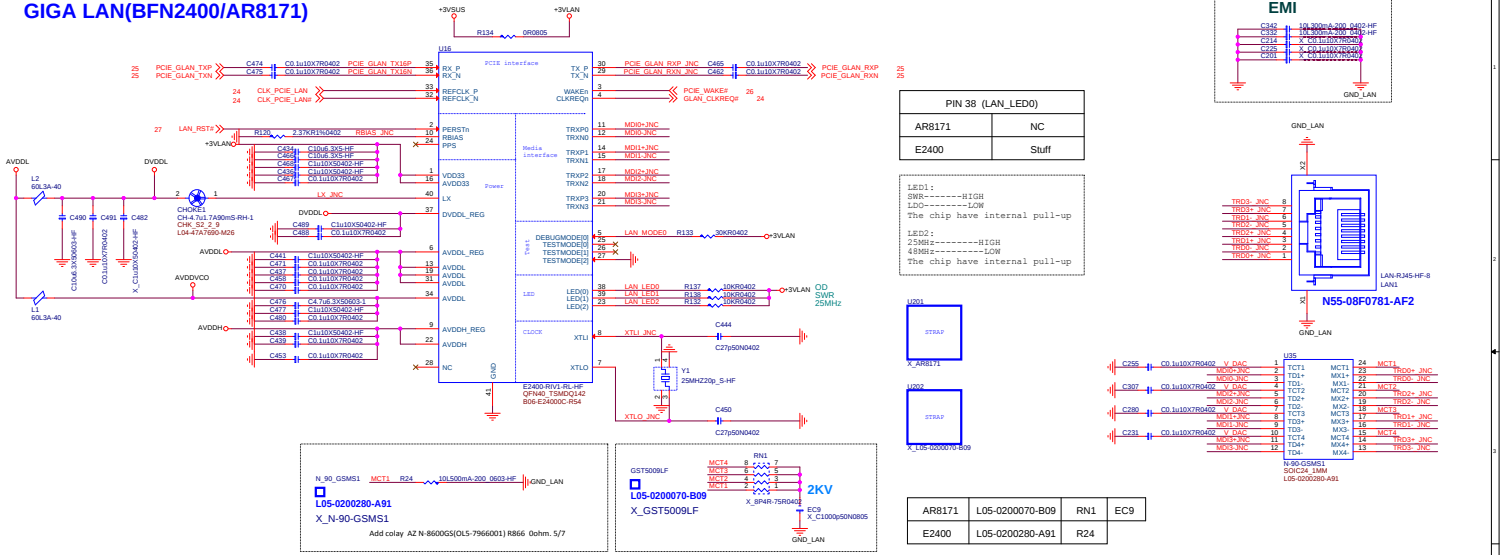
(Must used the gold fresh type)

RU20	RU21
	
E43-1205022-H29	E43-1205022-H29
RUBBER	RUBBER

03/21 1.0 Add E43-1205022-H29 臉搗

[illegible]

GIGA LAN(BFN2400/AR8171)



Vinafix.com

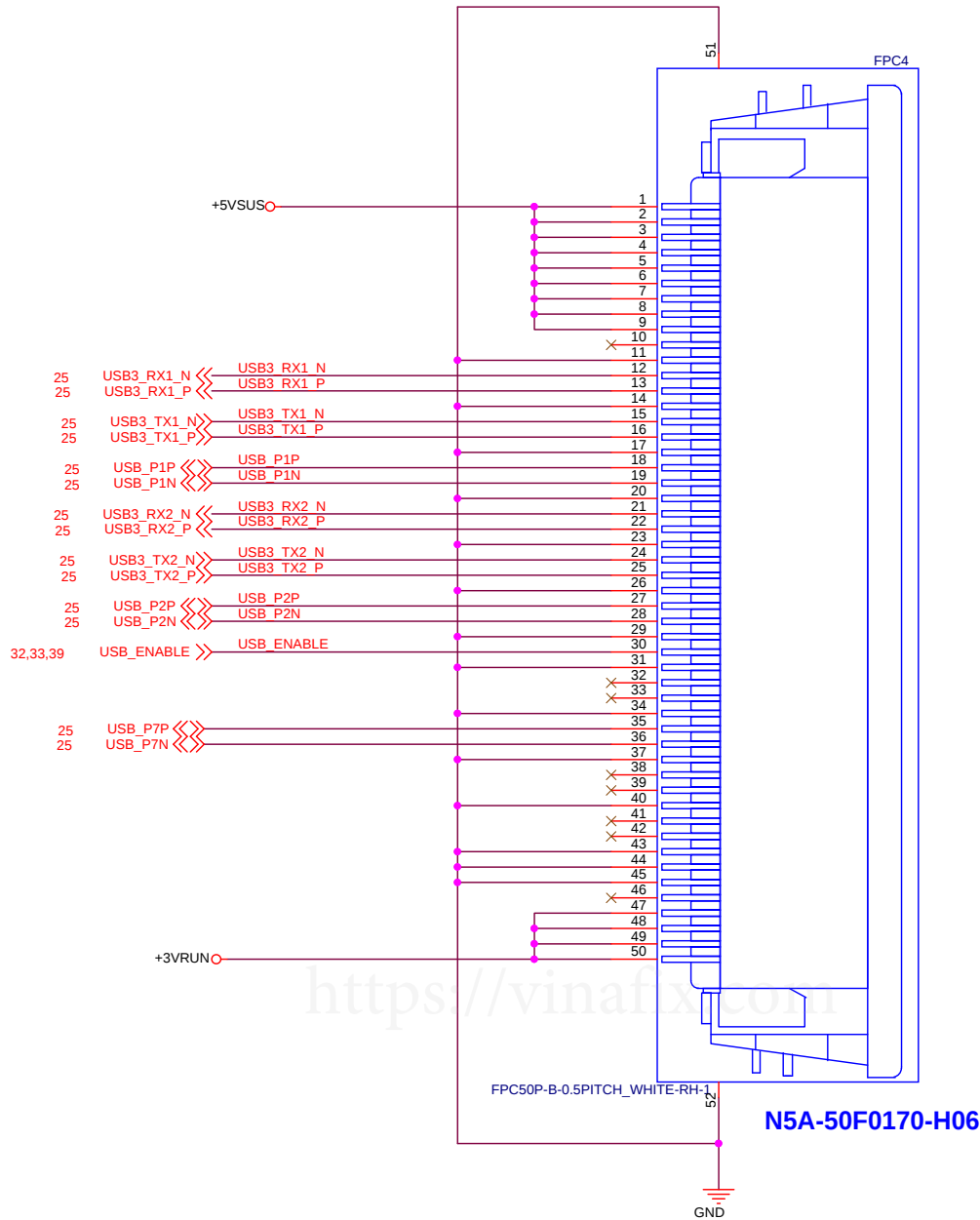
<https://vinafix.com>

msi MICRO-STAR INT'L CO., LTD.

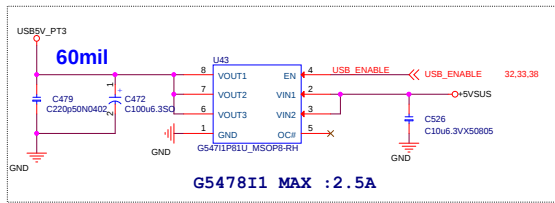
File: **GigaLAN (E2500)**

Rev: **MS-16P61**

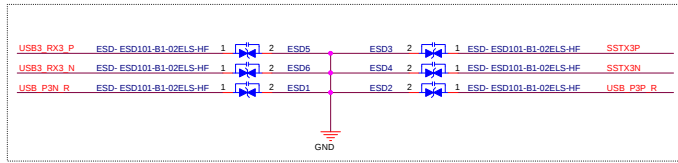
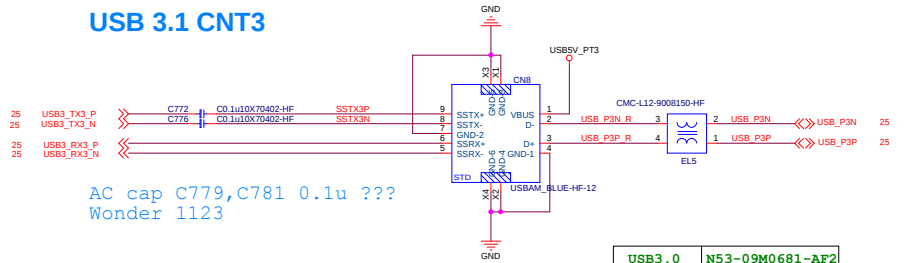
Date: **January 27, 2018** Sheet: **17** of **84**



msi		MICRO-STAR INT'L CO.,LTD.	
Title		USB 3.0 connector	
Size	Document Number	Rev	
Custom	MS-16P61	10	
Date:	Saturday, January 27, 2018	Sheet	38 of 64



USB 3.1 CNT3



USB3_0	N53-09M0681-AF2
USB3_0_LED	N53-13M0031-L06

msi MICRO-STAR INT'L CO.,LTD.	
Title	
USB 3.1 connector	
Size	Document Number
Custom	MS-16P61
Date	Saturday, January 27, 2018
Sheet	39 of 64
Rev	10

<https://vinafix.com>

Audio CODEC (ALC898/ALC892)

DVDD
Close Codec

AVDD5V

Close Pin25
Close Pin38

CODEC LDOOUT

EMITTER

SPK 2619

Keyboard LED

Internal Mic

EMI Close Codec

Pin 37 - VREF0

Pin	Signal	Notes
37	VREF0	NC
38	VREF0	NC
39	VREF0	NC
40	VREF0	NC
41	VREF0	NC
42	VREF0	NC
43	VREF0	NC
44	VREF0	NC
45	VREF0	NC
46	VREF0	NC
47	VREF0	NC
48	VREF0	NC
49	VREF0	NC
50	VREF0	NC
51	VREF0	NC
52	VREF0	NC
53	VREF0	NC
54	VREF0	NC
55	VREF0	NC
56	VREF0	NC
57	VREF0	NC
58	VREF0	NC
59	VREF0	NC
60	VREF0	NC
61	VREF0	NC
62	VREF0	NC
63	VREF0	NC
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66	VREF0	NC
67	VREF0	NC
68	VREF0	NC
69	VREF0	NC
70	VREF0	NC
71	VREF0	NC
72	VREF0	NC
73	VREF0	NC
74	VREF0	NC
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76	VREF0	NC
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83	VREF0	NC
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85	VREF0	NC
86	VREF0	NC
87	VREF0	NC
88	VREF0	NC
89	VREF0	NC
90	VREF0	NC
91	VREF0	NC
92	VREF0	NC
93	VREF0	NC
94	VREF0	NC
95	VREF0	NC
96	VREF0	NC
97	VREF0	NC
98	VREF0	NC
99	VREF0	NC
100	VREF0	NC

CODEC HDA SOUND

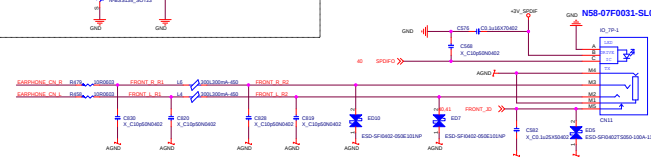
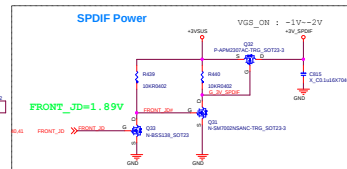
EMI (RADIATION SOLUTION)

ALC892 Codec Spec max=1.2Vrms
After Spec the codec output Vpp is 1.38V ,0.488Vrms

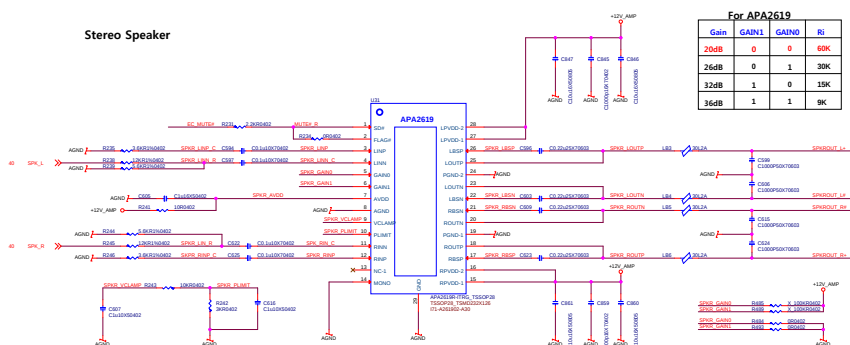
U35(APA2051) Pin23: gain set
5.1V*39K/(18K+39K)=3.489V
10dB = 3.48V/(R469:18K, R466:39K)
dB=20Log(Vo/Vi)
/E spec = 2W/40hm
10dB =20Log 3.16, Vout = 0.488Vrms *3.16 =1.54Vrms
Pow=(1.54*1.54)/4=0.59W

Pin 37 - VREF0

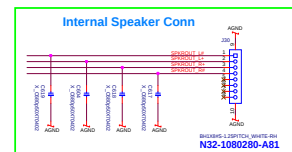
Pin	Signal	Notes
37	VREF0	NC
38	VREF0	NC
39	VREF0	NC
40	VREF0	NC
41	VREF0	NC
42	VREF0	NC
43	VREF0	NC
44	VREF0	NC
45	VREF0	NC
46	VREF0	NC
47	VREF0	NC
48	VREF0	NC
49	VREF0	NC
50	VREF0	NC
51	VREF0	NC
52	VREF0	NC
53	VREF0	NC
54	VREF0	NC
55	VREF0	NC
56	VREF0	NC
57	VREF0	NC
58	VREF0	NC
59	VREF0	NC
60	VREF0	NC
61	VREF0	NC
62	VREF0	NC
63	VREF0	NC
64	VREF0	NC
65	VREF0	NC
66	VREF0	NC
67	VREF0	NC
68	VREF0	NC
69	VREF0	NC
70	VREF0	NC
71	VREF0	NC
72	VREF0	NC
73	VREF0	NC
74	VREF0	NC
75	VREF0	NC
76	VREF0	NC
77	VREF0	NC
78	VREF0	NC
79	VREF0	NC
80	VREF0	NC
81	VREF0	NC
82	VREF0	NC
83	VREF0	NC
84	VREF0	NC
85	VREF0	NC
86	VREF0	NC
87	VREF0	



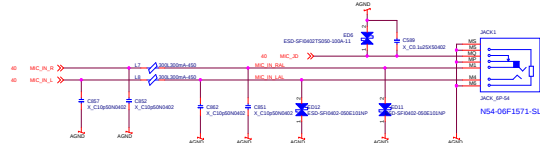
Stereo Speaker



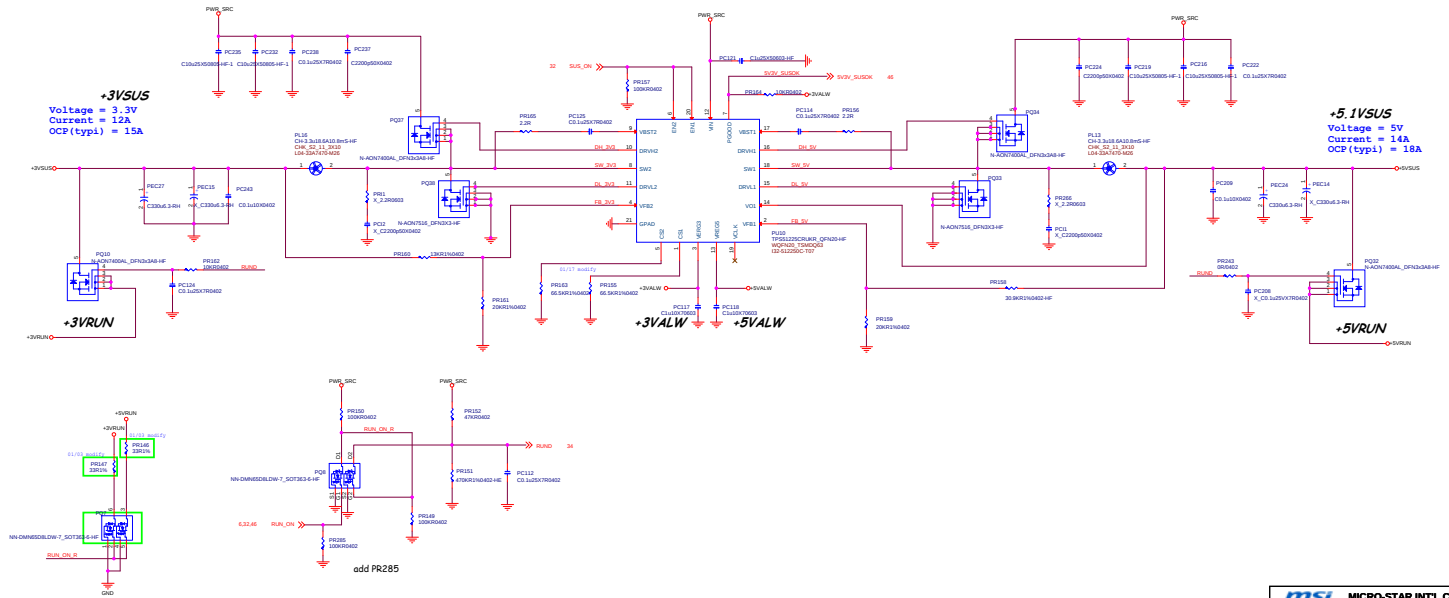
Gain	GAIN1	GAIN2	RS
20dB	0	0	49K
26dB	0	1	30K
32dB	1	0	19K
36dB	1	1	9K

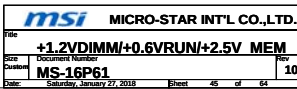


CODEC	FP
L	-
R	-
TP	-
B	-
CS	-
FS	-
FS	-
FS	-
FS	-
FS	-

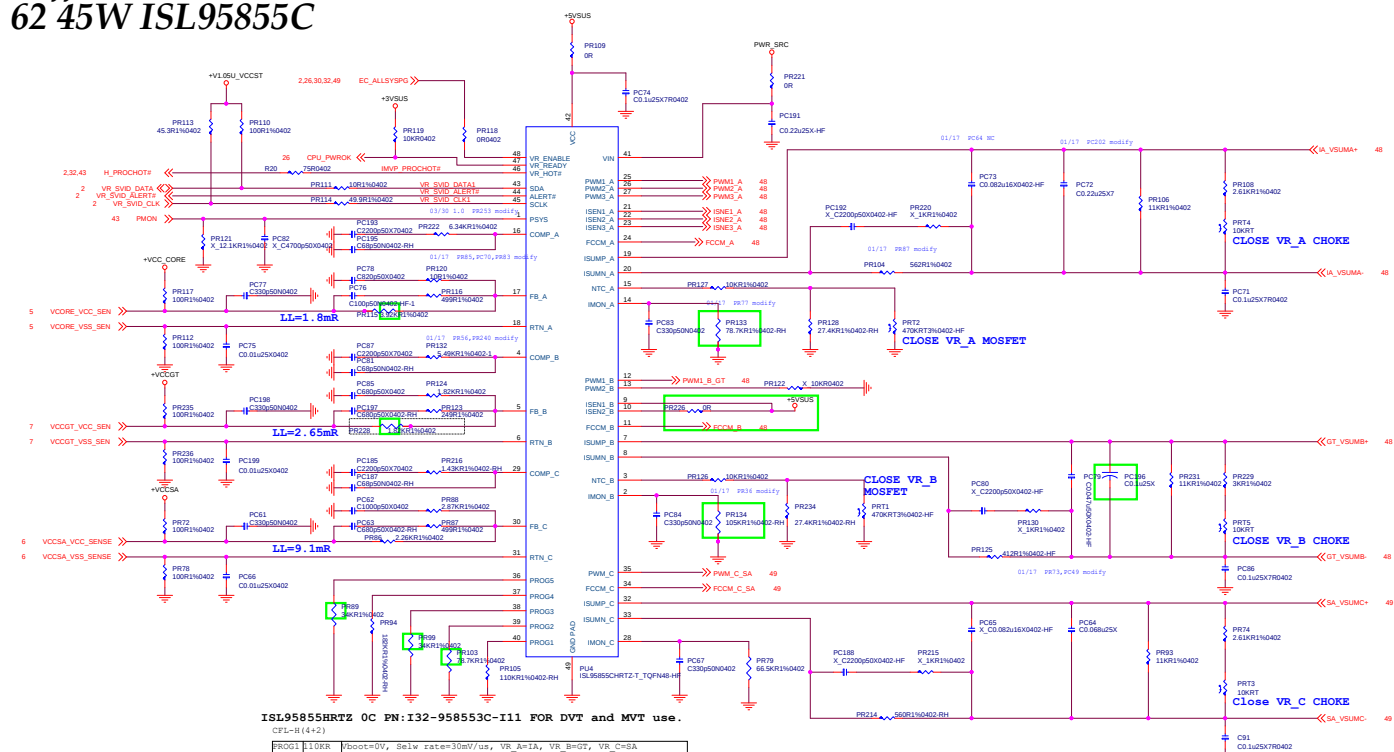


<https://vinafix.com>





Coffee Lake H-line
62 45W ISL95855C

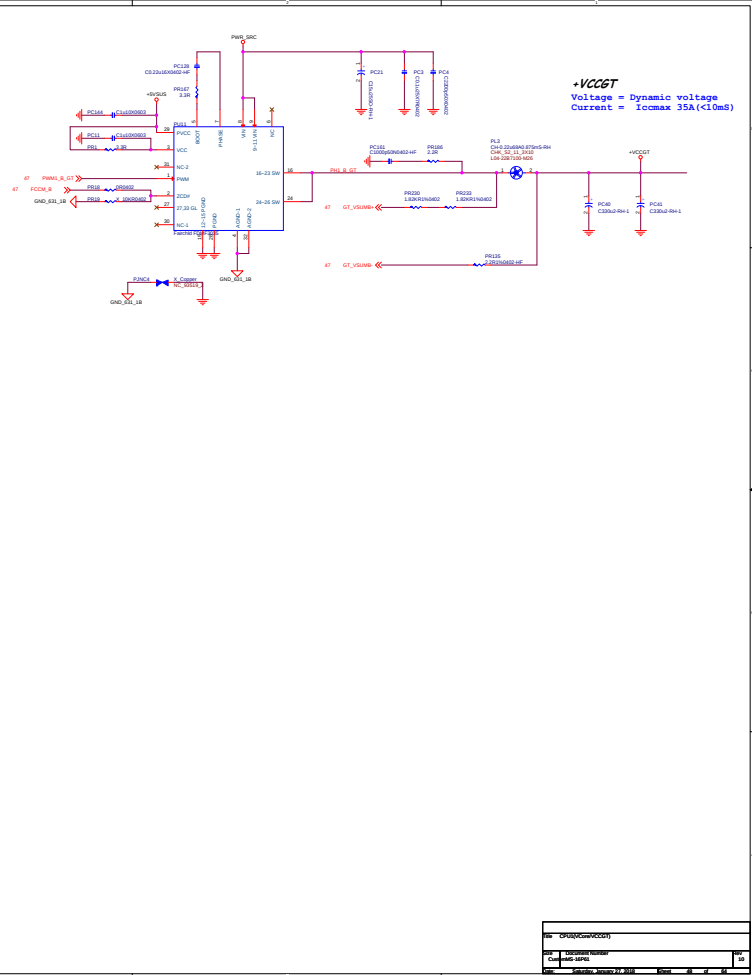


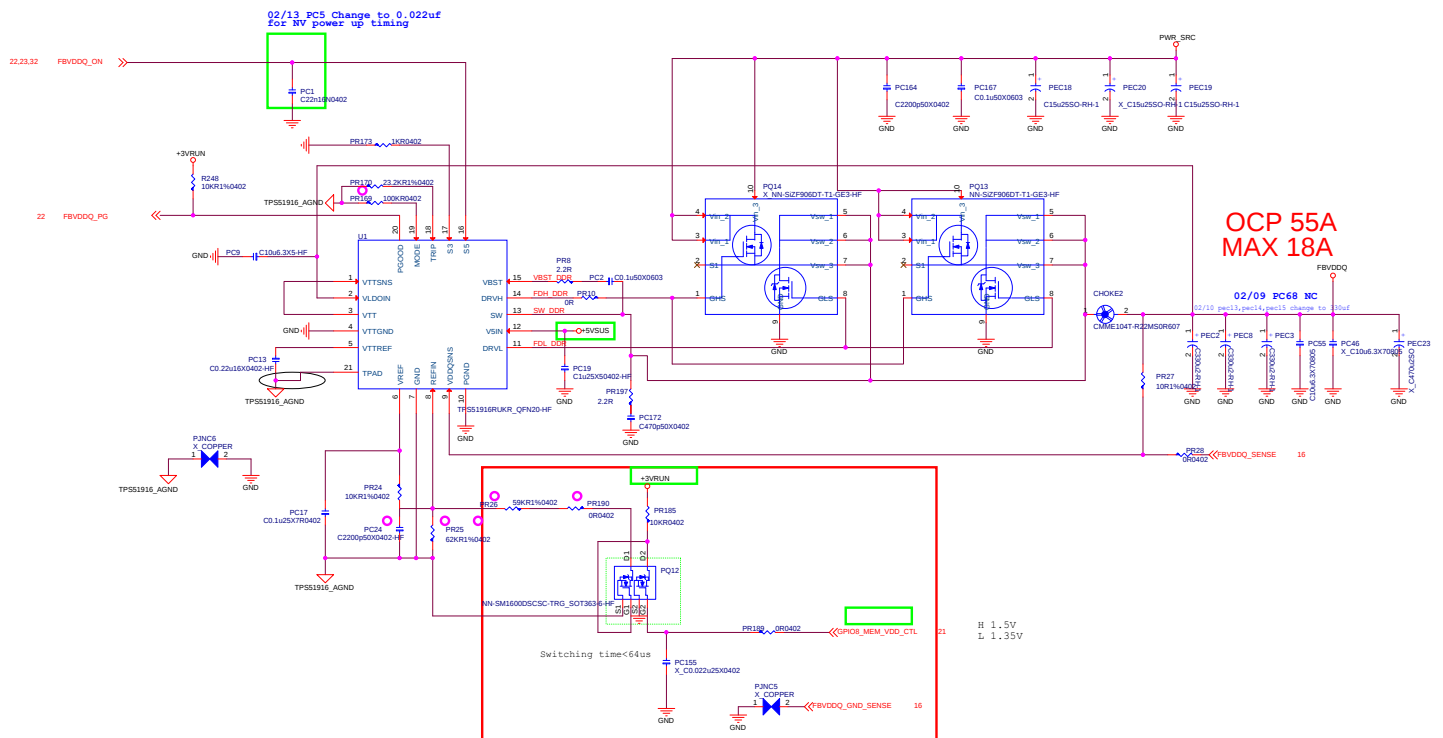
ISL95855HRTZ 0C PN:I32-958553C-I11 FOR DVT and MVT use.

CFL-H(4+2)

PROG1	110KR	Vboot=0V, Selw rate=30mV/us, VR_A=IA, VR_B=GI, VR_C=SA
PROG2	78.7KR	IMAX VR_A=128A, VR_A PSII=1FH
PROG3	34KR	IMAX VR_B=70A, DROOF VR_B Active
PROG4	182KR	DROOF VR_A Active, DROOF VR_C Active, VR_A VR_B Frequency=750kHz
PROG5	34KR	IMAX VR_C=17A, Frequency=450kHz

File									
CPU Power (ISL95855)									
Size	Document Number								Rev
Customer	MS-16P61								10
Date:	Submitted:	January 27, 2019	Elapsed:	47	ms	6.4			

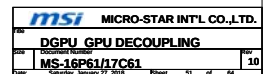


FBVDDQ

 MICRO-STAR INT'L CO.,LTD.	
File DGPU POWER FBVDDQ	
Size	Document Number MS-16P61
Date	Sheet 50 of 64 Rev 10

EDP-Peak 90A
EDP-Con 47A

VBoot:0.8V
Vmin:0.5V / Vmax:1.25V



DGPU POWER / UP1666P DGPU POWER NVVDDS

EDP-Peak 74A
EDP-Con 28A

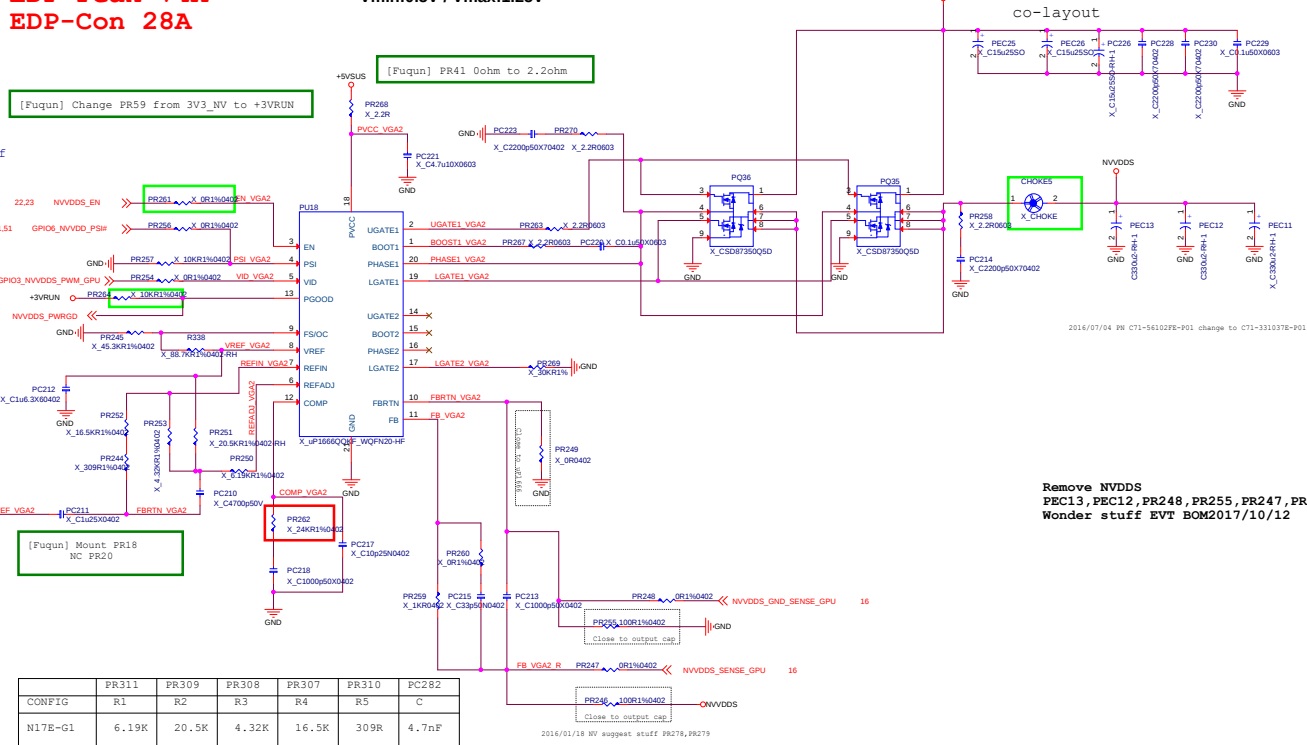
VBoot:0.8V
Vmin:0.5V / Vmax:1.25V

[Fuqun] Change PR59 from 3V3_NV to +3VRUN

[Fuqun] PR41 0ohm to 2.2ohm

[Fuqun] Mount FR18
NC PR20

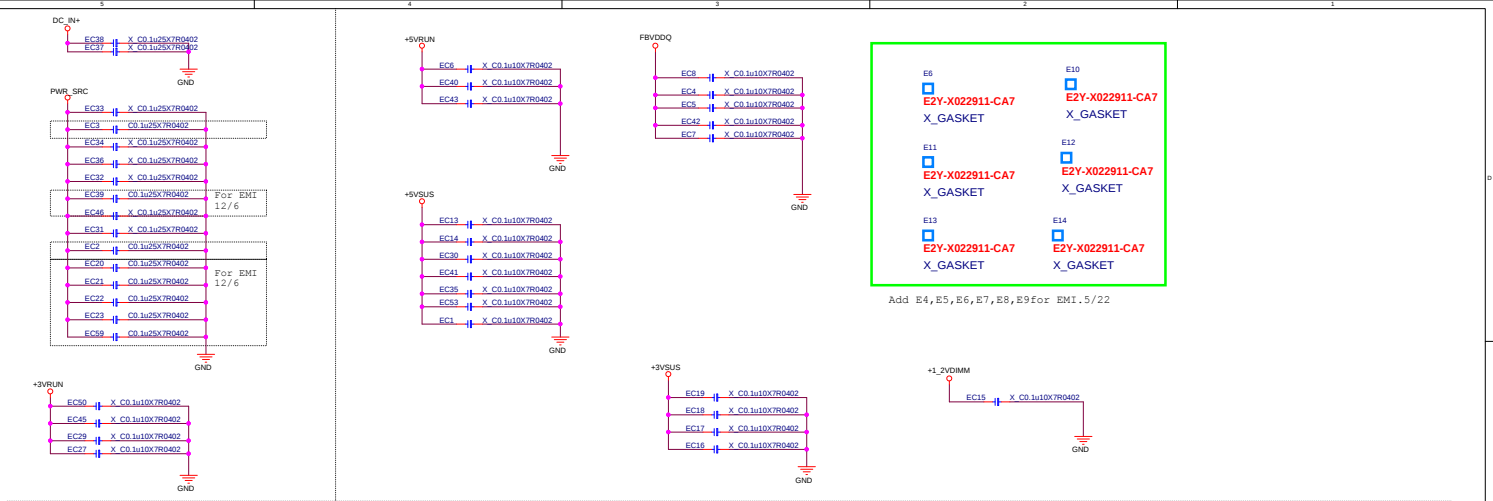
	PR311	PR309	PR308	PR307	PR310	PC282
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	4.7nF



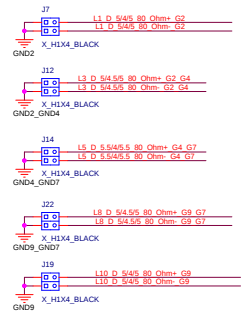
2016/07/04 PW C71-56102PR-P01 change to C71-331037E-P01

Remove NVVDDS
PEC13, PEC12, PR248, PR255, PR247, PR246
Wonder stuff EVT BOM2017/10/12

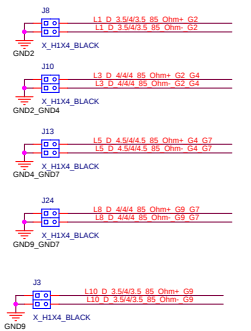
2016/01/18 NV suggest stuff PR278, PR279



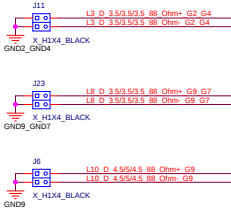
80 OHM / CLK/WCK/USB3.1



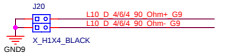
85 OHM /SATA /PCIE/ EDP/CNVI USB /HDMI/DP/DMI/CLK/PEG



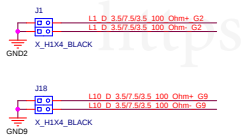
88 OHM /DDR4 CLK/DQS



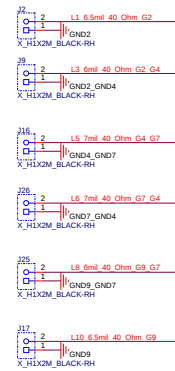
90 OHM USB 3.1 MUX/XTLIN/OUT



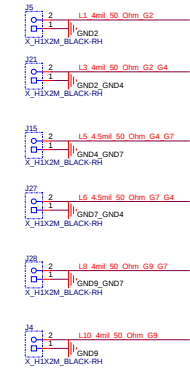
100 OHM LAN



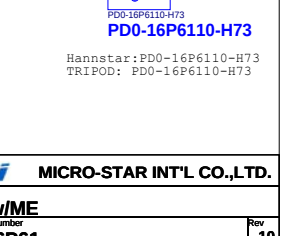
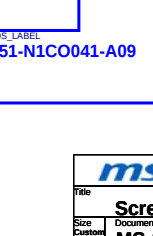
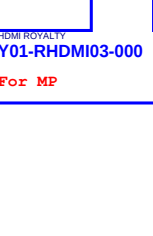
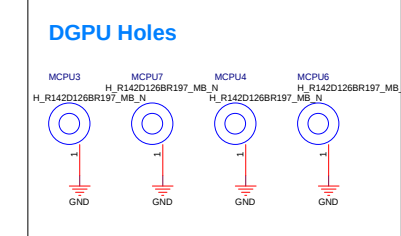
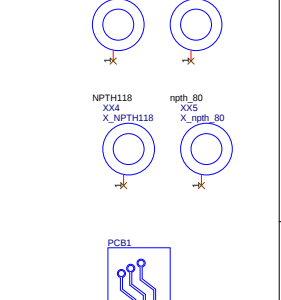
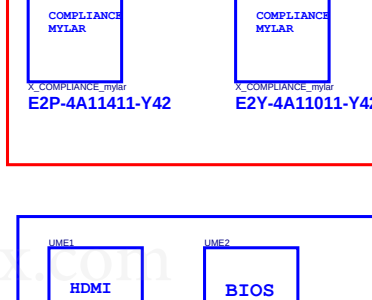
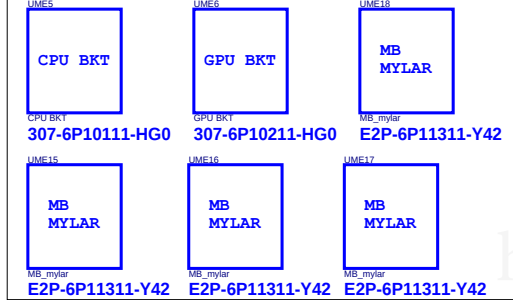
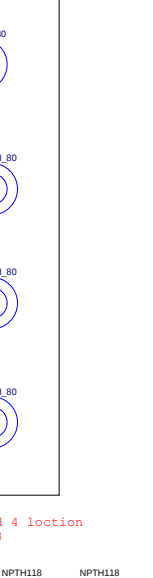
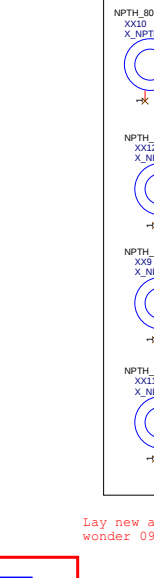
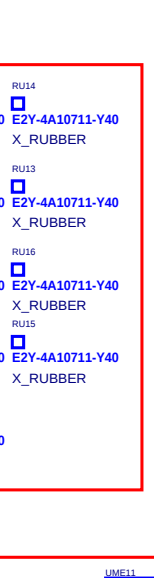
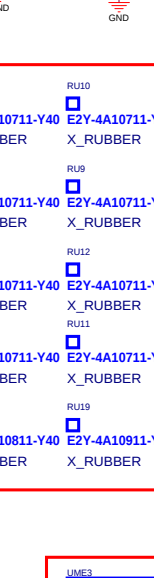
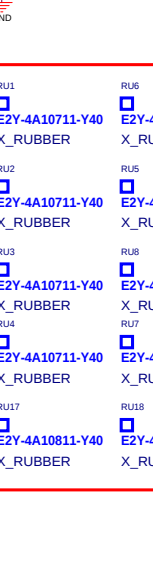
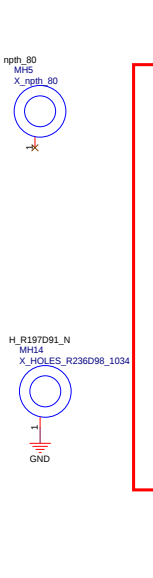
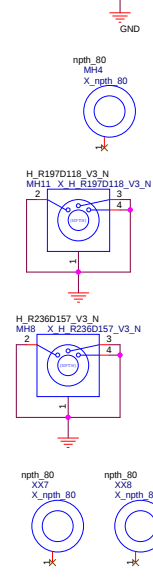
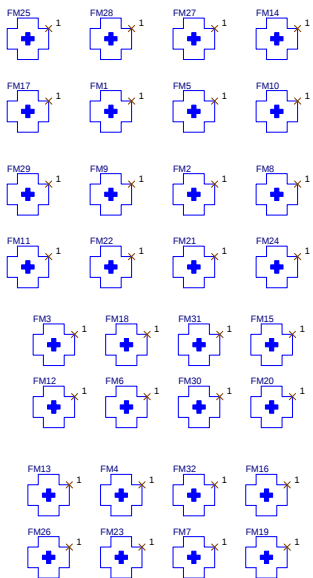
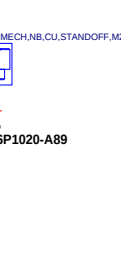
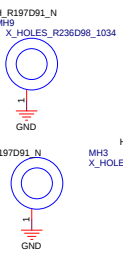
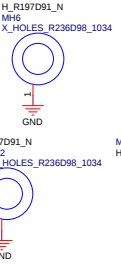
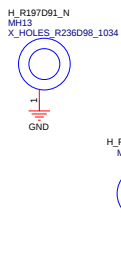
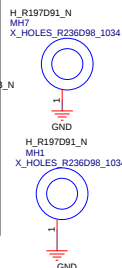
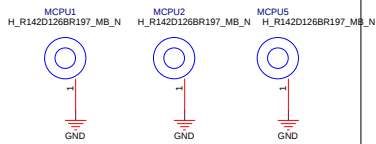
40 OHM DDR4 :CTL/ADD GPU:FBA/FBB DQ DB,



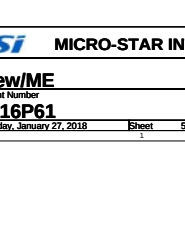
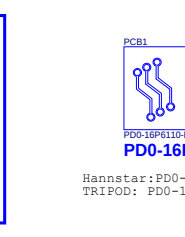
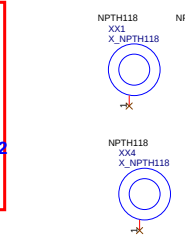
500OHM DDR4:RST/DQ/ECC/HPD/STRAP/SPI



CPU Holes

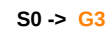


Lay new add 4 location wonder 0913



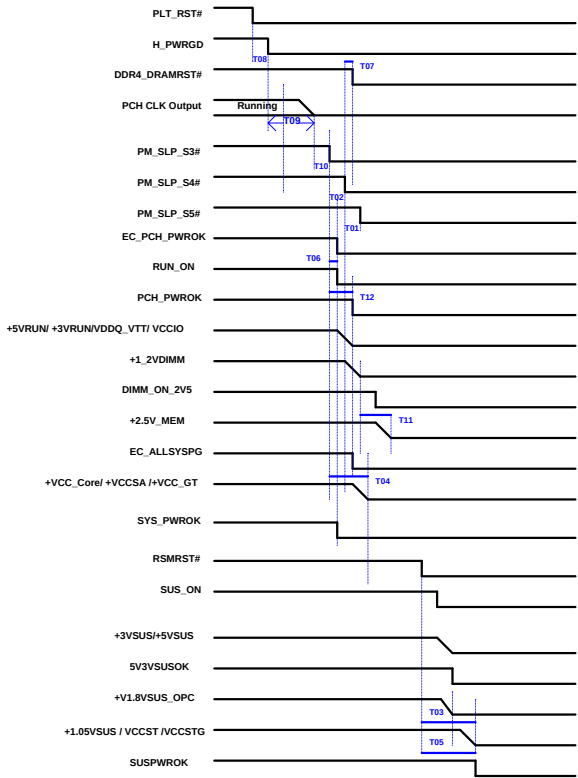
msi MICRO-STAR INT'L CO.,LTD.	
Title	Screw/ME
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G3 -> S0



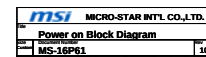
Power down Sequence

S0 -> G3

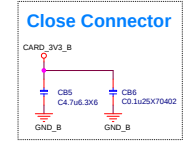
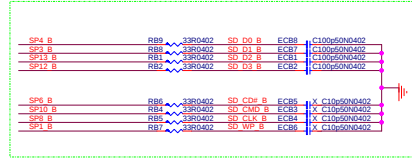
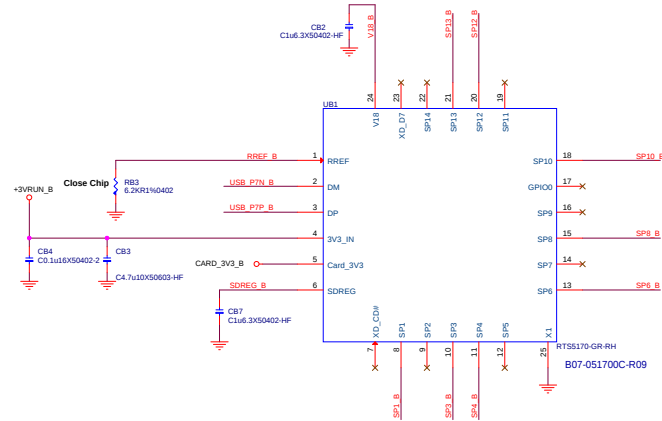


	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

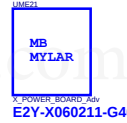
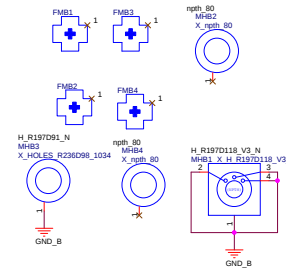
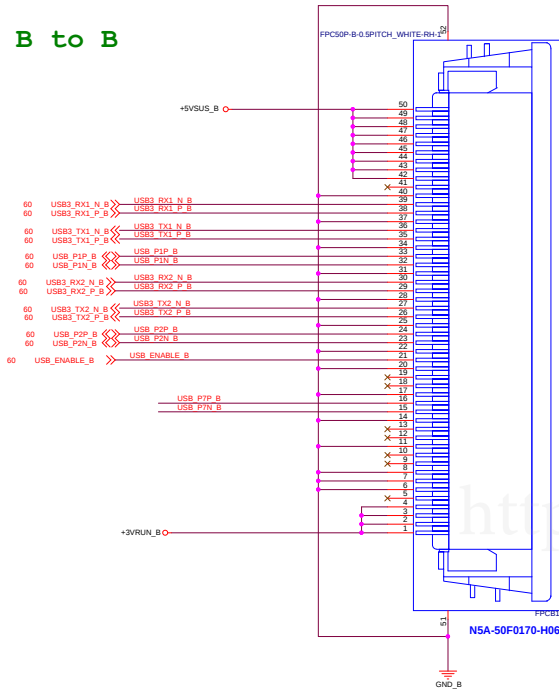
ref DG Chapter45 Power Sequencing Spec



CardReader (RTS5170)



B to B



PD0-16P6B10-H73
Hannstar: PD0-16P6B10-H73
TRIPOD: PD0-16P6B10-T53



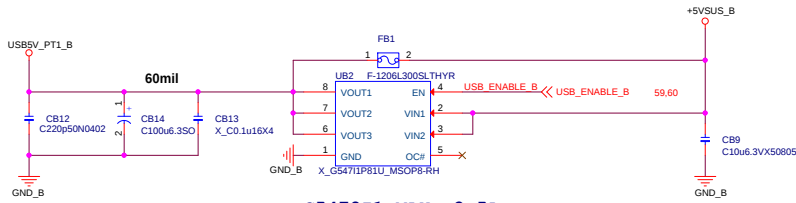
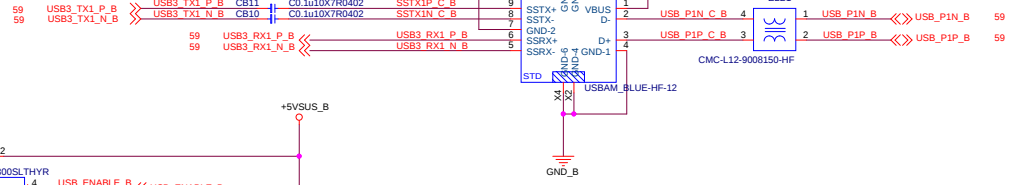
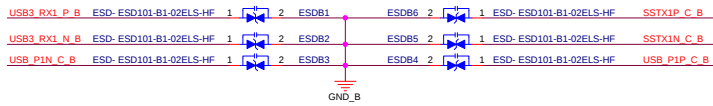
MB MYLAR
E2Y-X060211-G40

Title			
BICard reader/RTB CONN			
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USB2.0/USB 3.1 CNT1

16P6上件

USB3.0	N53-09M0681-AF2
USB3.0_LED	N53-13M0031-L06

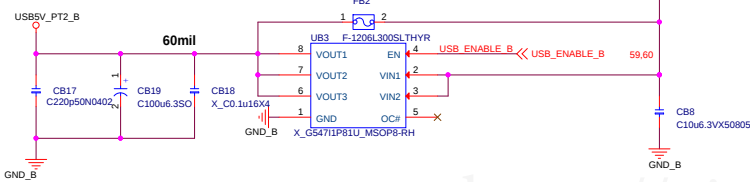
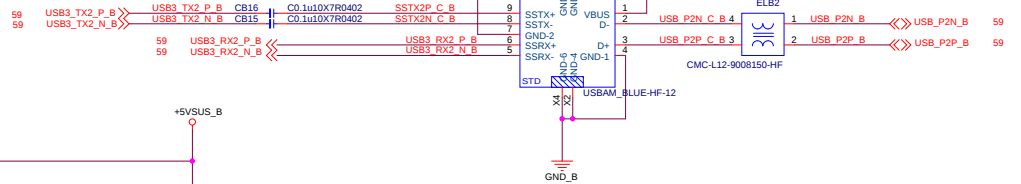
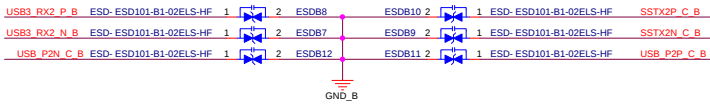


G5478I1 MAX :2.5A

USB2.0/USB 3.1 CNT2

16P6上件

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USB3.0_LED	N53-13M0031-L06

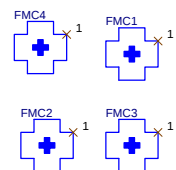


G5478I1 MAX :2.5A

<https://vinafix.com>

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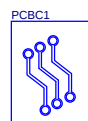
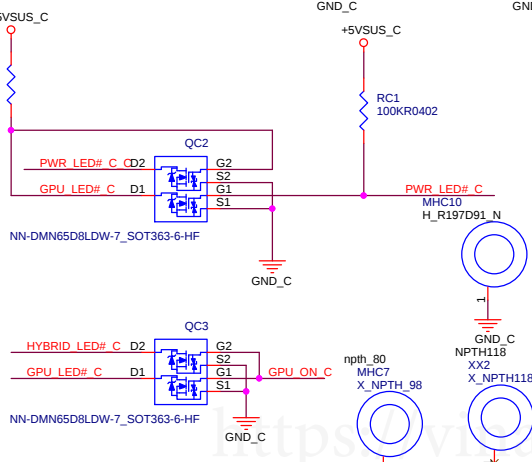
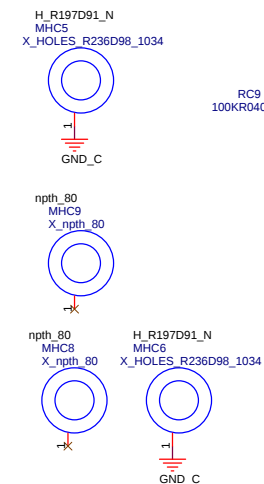
Power LED



Cooler led and dragon led DEL

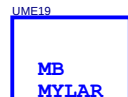
Power Switch

Control PWR LED



PD0-16P6C10-H73

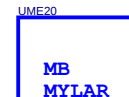
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TRIPOD: PD0-16P6C10-T53



MB MYLAR

POWER_BOARD_mylar

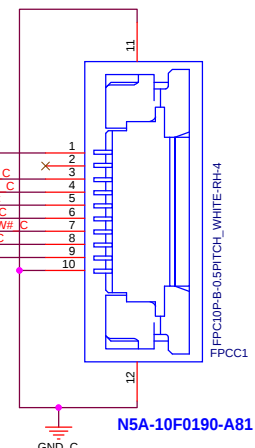
E2Y-7C40211-Y42



MB MYLAR

POWER_BOARD_mylar

E2P-7C60111-Y42



N71-0101630-D02

N71-0101630-D02

N5A-10F0190-A81

Title			
[C]Power Switch			
Size	Custom	Document Number	MS-16P6C
Customer		teknisi indonesia	
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LEDD1
LED04-WO-20mA3.15V30mA A2.4V_1516-RH

Current 30mA

+5VSUS_D

RD4 2.2KR

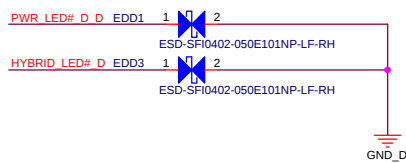
PWR_LIGHT_D

RD3 2.2KR

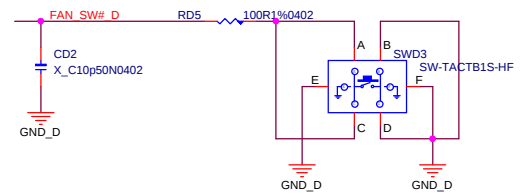
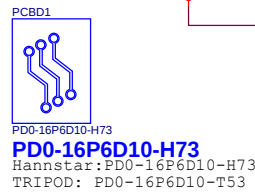
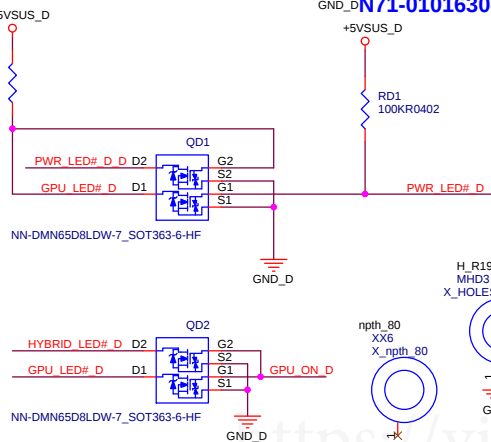
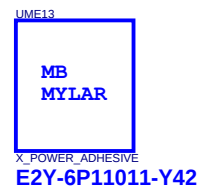
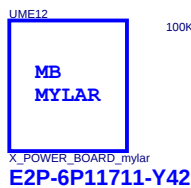
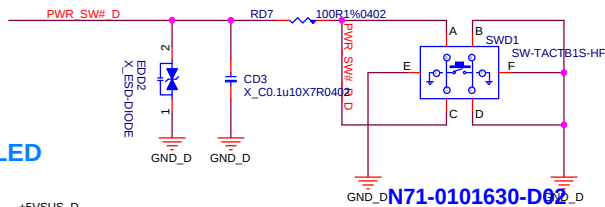
HYBRID_LIGHT_D

PWR_LED#_D

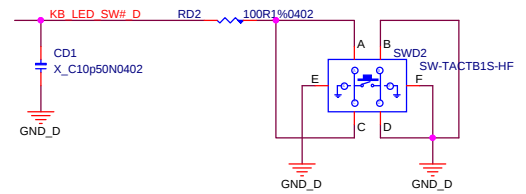
HYBRID_LED#_D



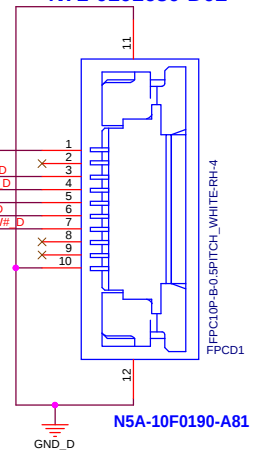
Control PWR LED



N71-0101630-D02



N71-0101630-D02

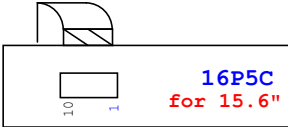


N5A-10F0190-A81

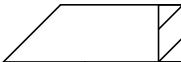
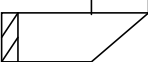
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Size	Document Number	10	Rev
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TOP

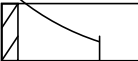
16P51



Power switch



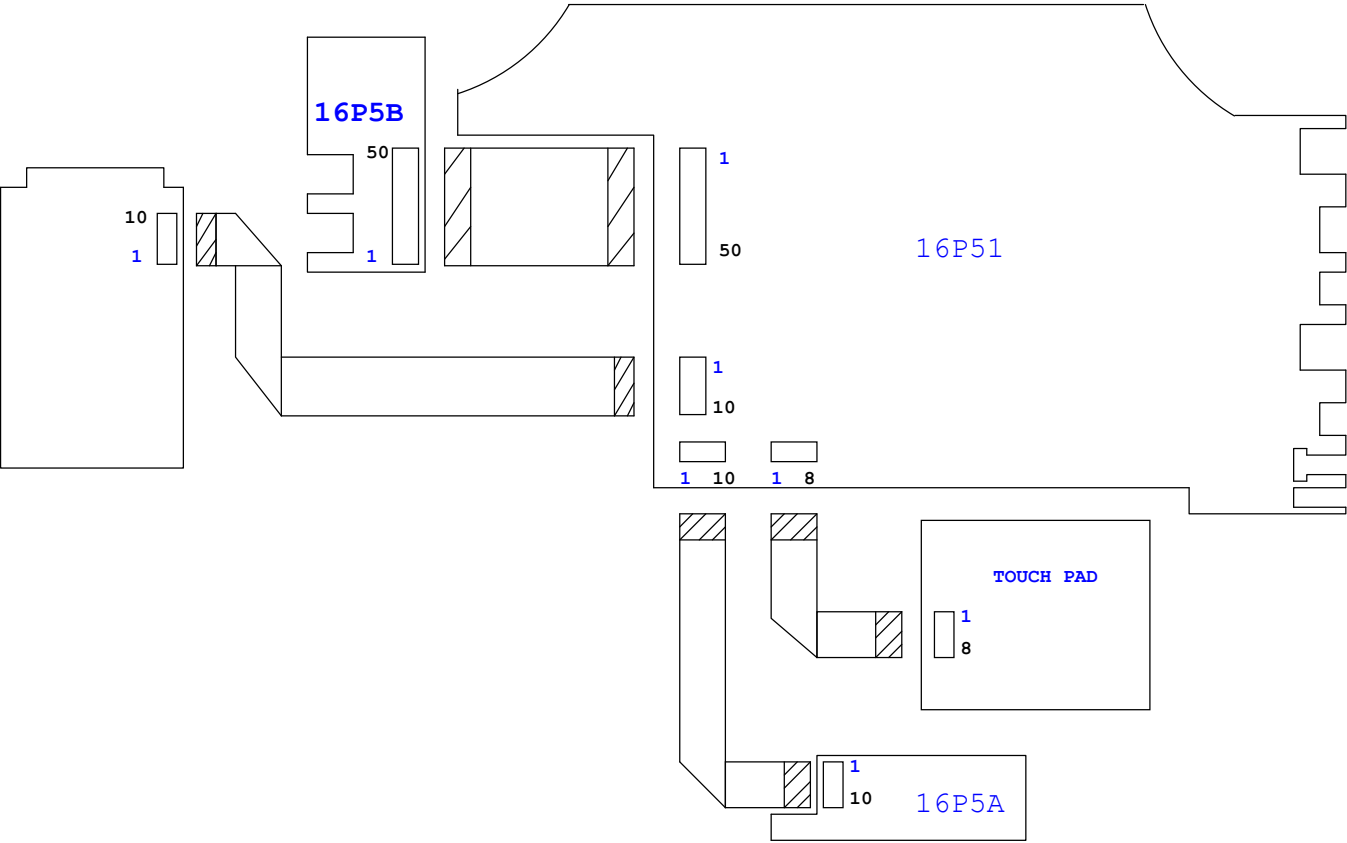
Power switch



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TOP VIEW		
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Bottom VIEW



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Bottom VIEW			
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